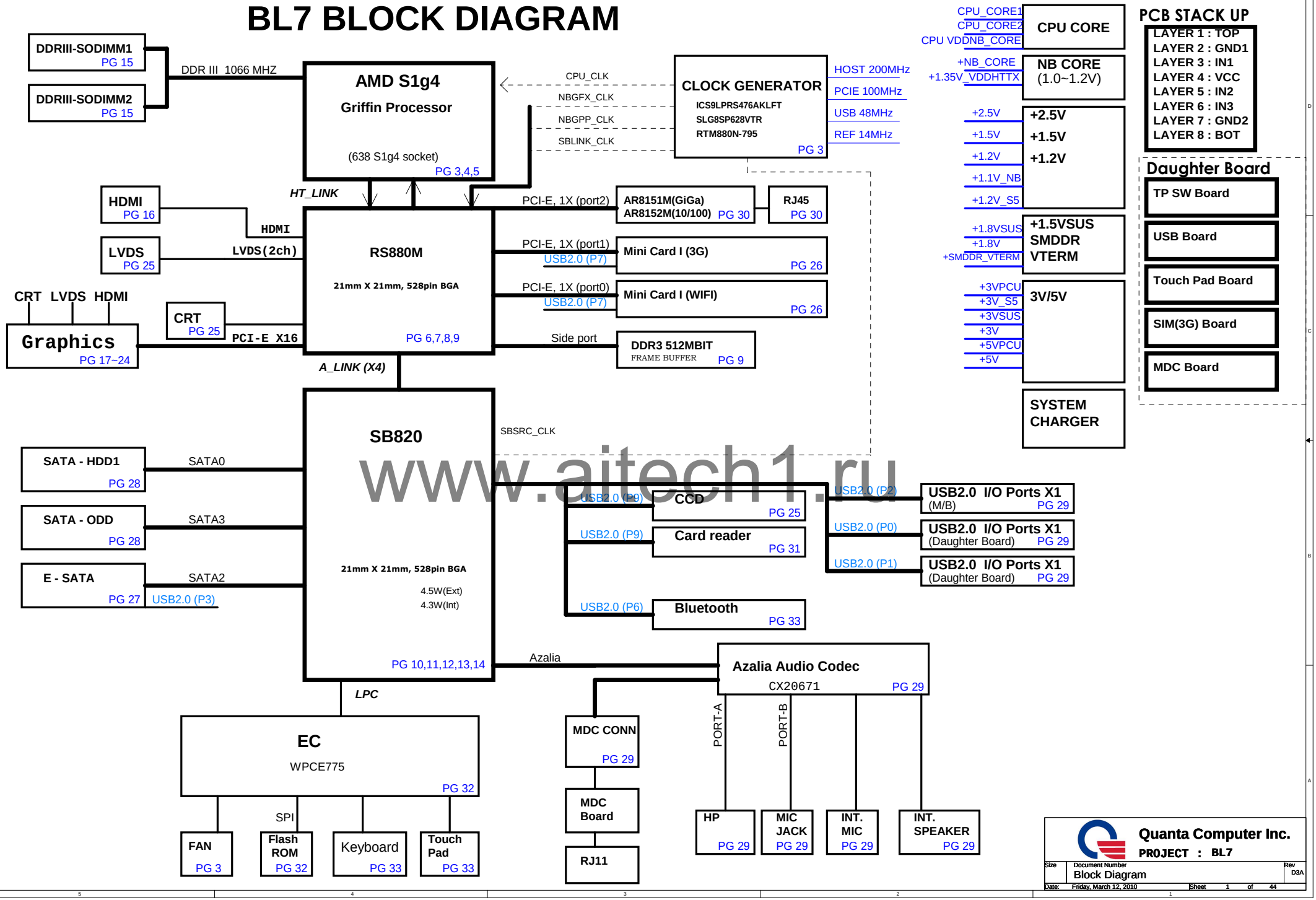
BL7 BLOCK DIAGRAM



PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND1
LAYER 3 : IN1
LAYER 4 : VCC
LAYER 5 : IN2
LAYER 6 : IN3
LAYER 7 : GND2
LAYER 8 : BOT

Daughter Board

- TP SW Board
- USB Board
- Touch Pad Board
- SIM(3G) Board
- MDC Board

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PROJECT : BL7

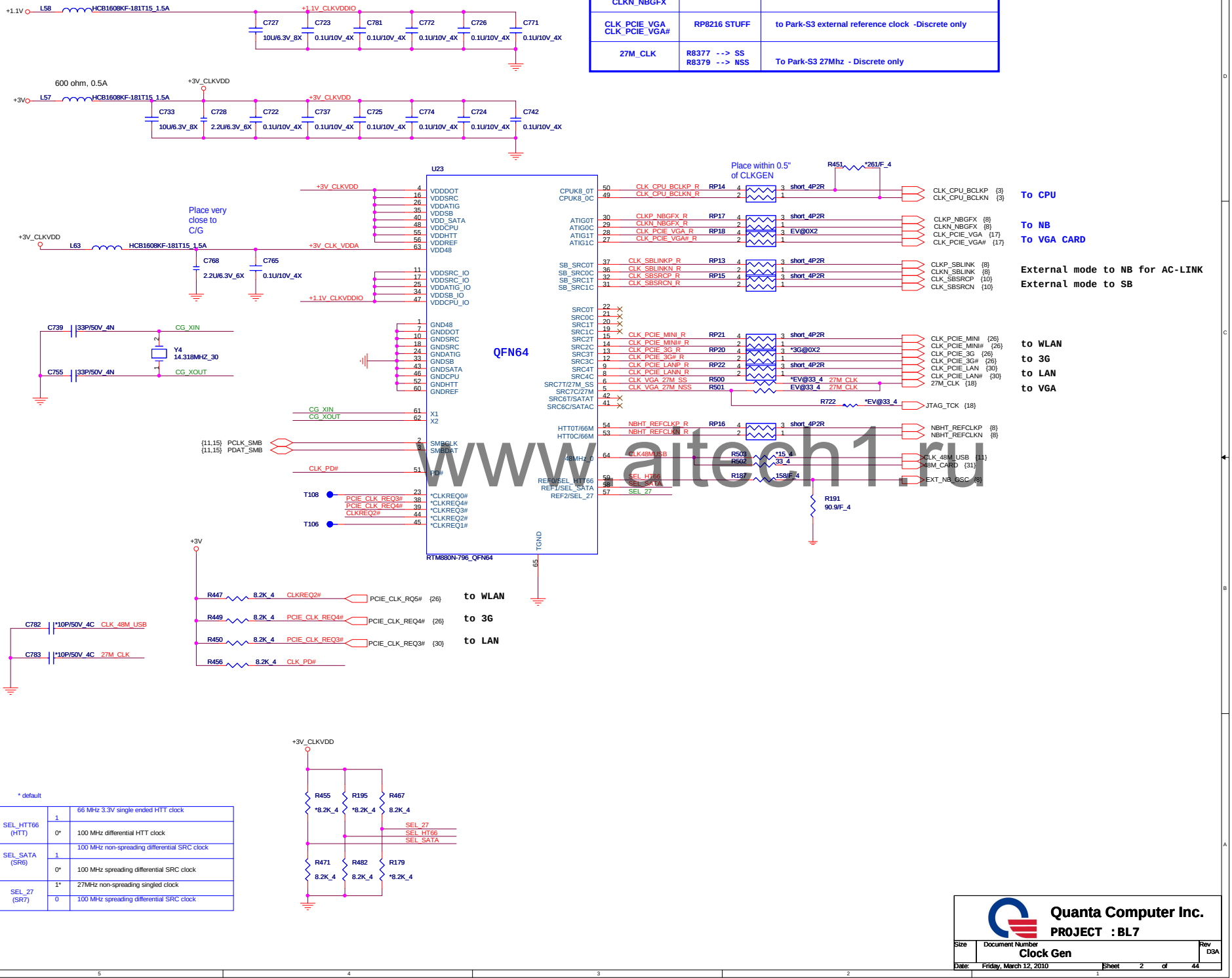
Size	Document Number	Rev
	Block Diagram	D3A

Date: Friday, March 12, 2010 Sheet 1 of 44

CLOCK GENERATOR

02

CLOCKS name	Discrete	Clock pin function
CLKP_NBGFX CLKN_NBGFX	RP8217 STUFF	to NB for VGA reference clock
CLK_PCIE_VGA CLK_PCIE_VGA#	RP8216 STUFF	to Park-S3 external reference clock -Discrete only
27M_CLK	R8377 --> SS R8379 --> NSS	To Park-S3 27Mhz - Discrete only



* default

SEL_HTT66 (HTT)	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA (SR6)	1	100 MHz non-spreading differential SRC clock
	0*	100 MHz spreading differential SRC clock
SEL_27 (SR7)	1*	27MHz non-spreading singled clock
	0	100 MHz spreading differential SRC clock

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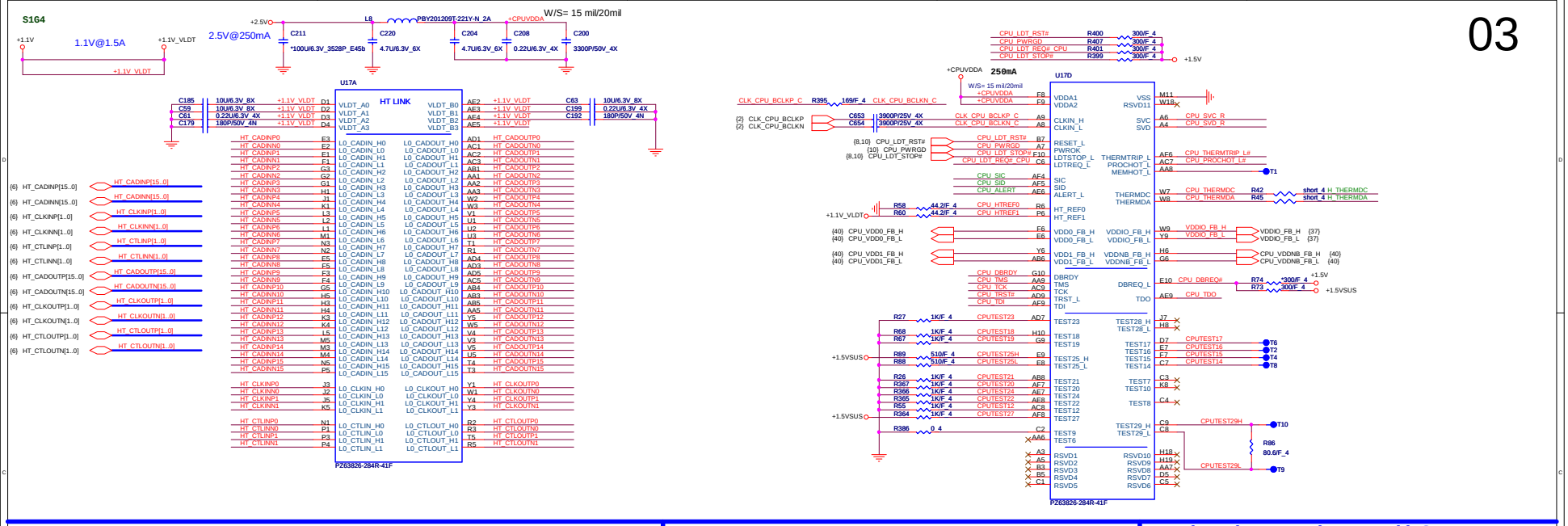
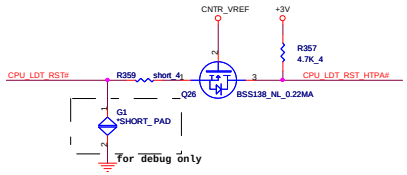
PROJECT : BL7

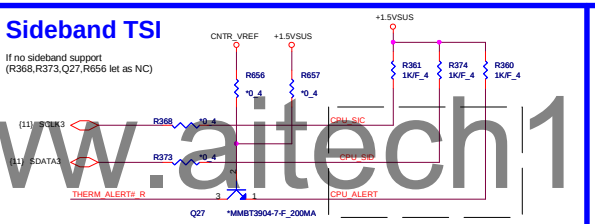
Size	Document Number	Rev
	Clock Gen	D3A
Date: Friday, March 12, 2010	Sheet 2 of 44	



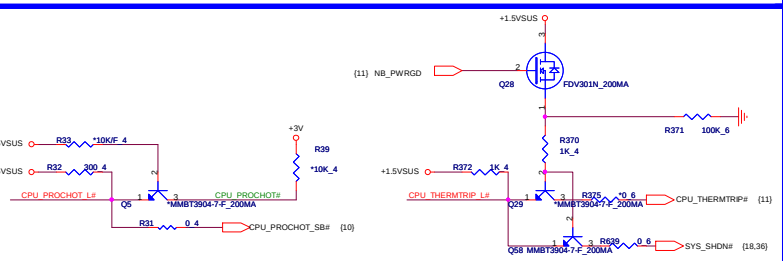


Sideband TSI

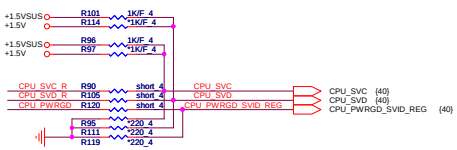
If no sideband support
(R368,R373,Q27,R656 let as NC)



HDT(Hardware Debug Tool) Connector



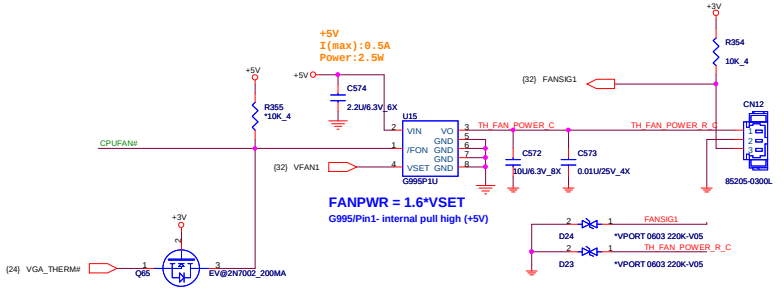
Serial VID



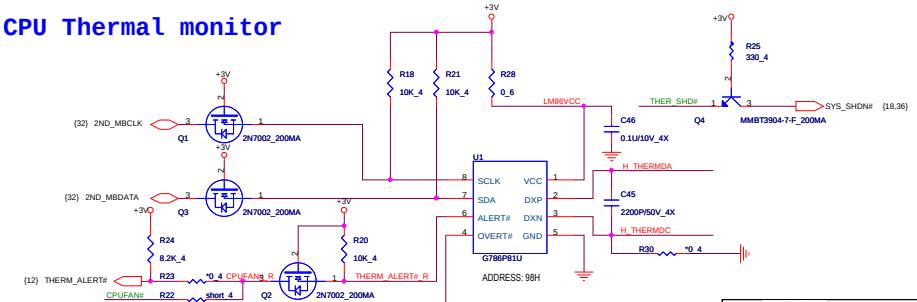
VFIX MODE — VID Override Circuit

SVC	SVD	Voltage Output
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

CPU FAN



CPU Thermal monitor



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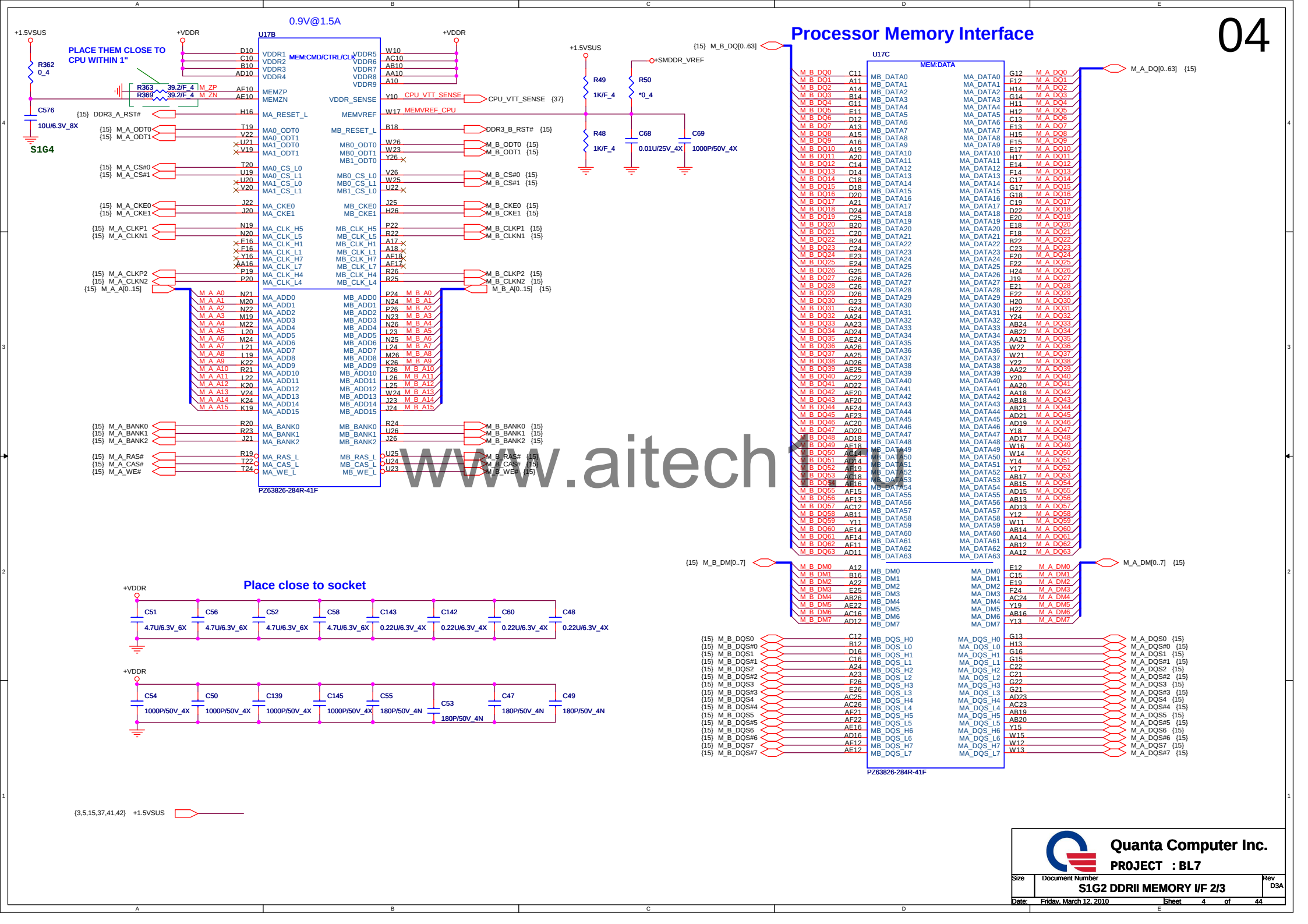
Quanta Computer Inc.
PROJECT : BL7

Size	Document Number	Rev
	S1G2 HT,CTL I/F 1/3	D3A

Date: Friday, March 12, 2010 Sheet 3 of 44


Processor Memory Interface
04
0.9V@1.5A
PLACE THEM CLOSE TO CPU WITHIN 1"
U17B
MEM:CMD/CTRL/CLK
PZ63826-284R-41F
U17C
MEM:DATA
PZ63826-284R-41F
Place close to socket
S1G4
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Quanta Computer Inc.
PROJECT : BL7
Size
Document Number
S1G2 DDRII MEMORY I/F 2/3
Rev
D3A
Date: Friday, March 12, 2010
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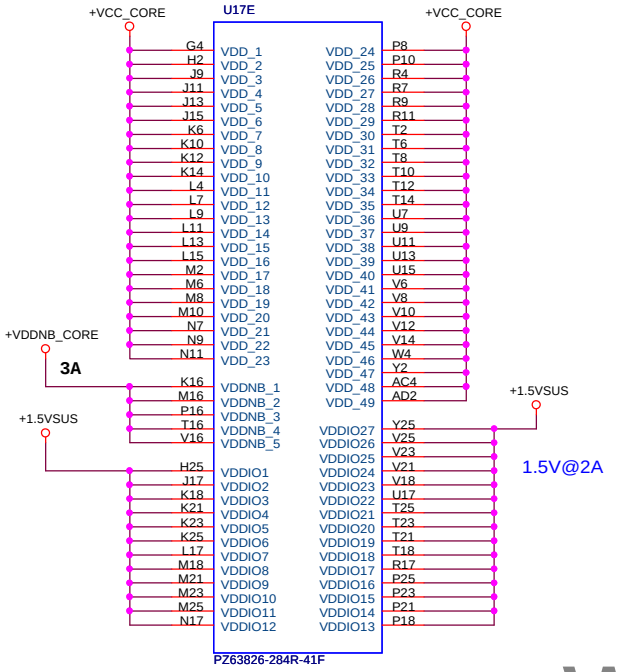

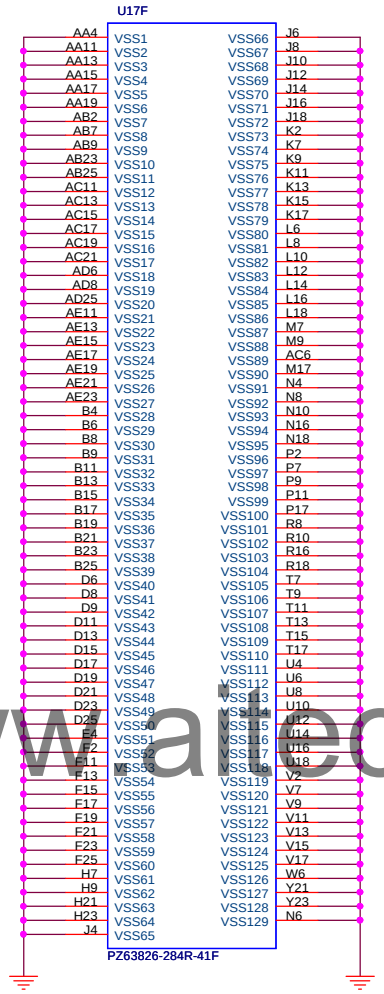

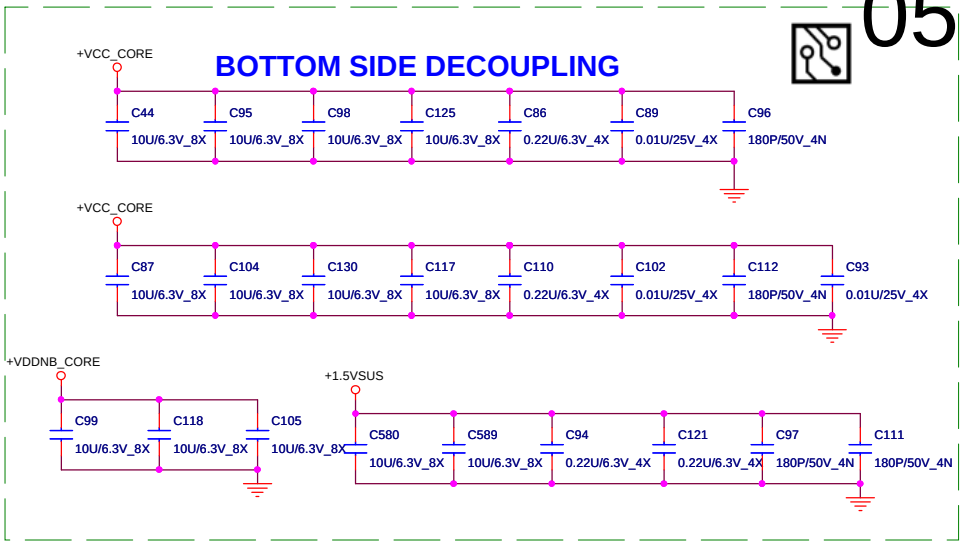

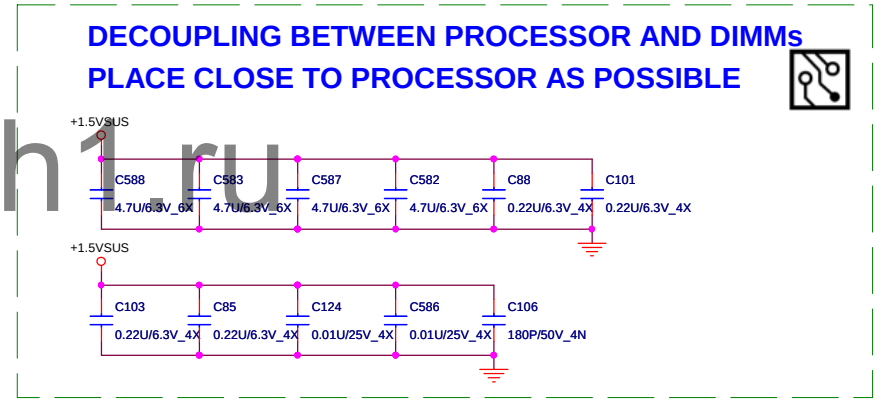

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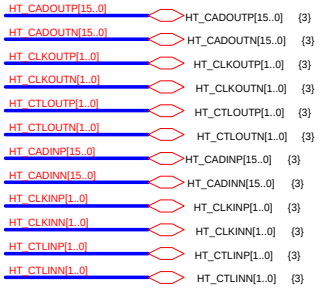
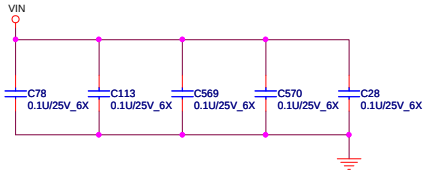
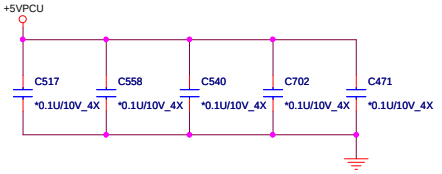
PROJECT : BL7

Size	Document Number	Rev
	S1G2 PWR & GND 3/3	D3A
Date: Friday, March 12, 2010	Sheet 5 of 44	







Memory Side Port

This block is for UMA only . Discrete can remove all component

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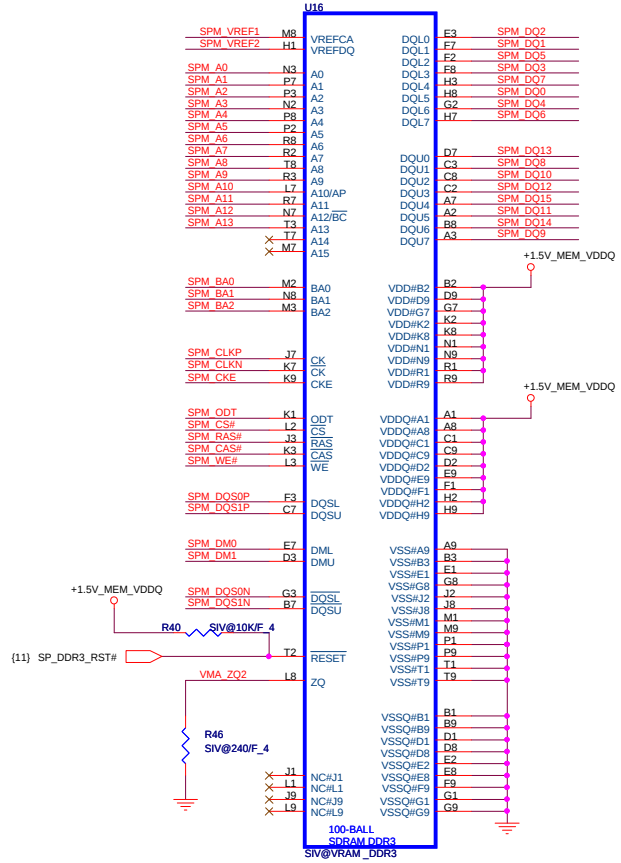

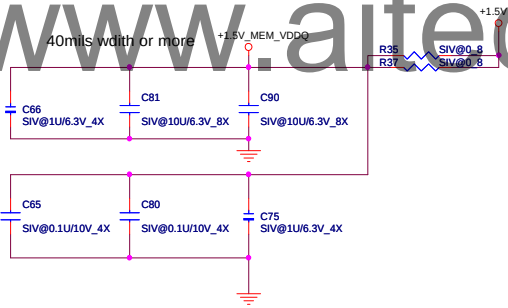

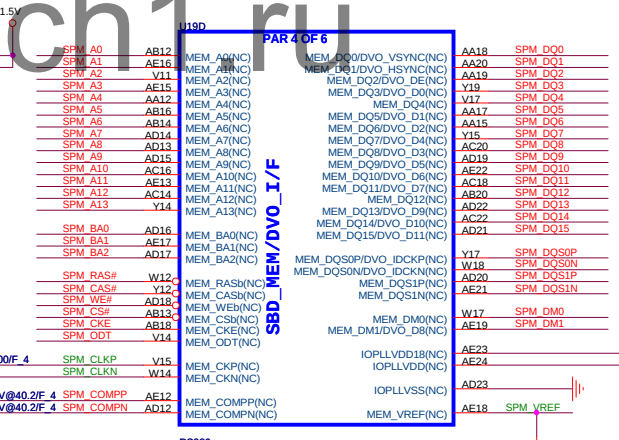

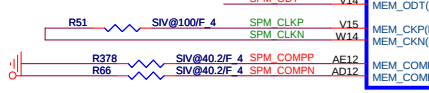

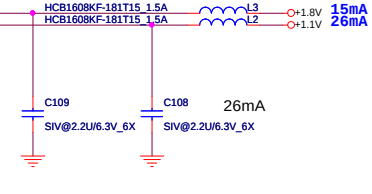

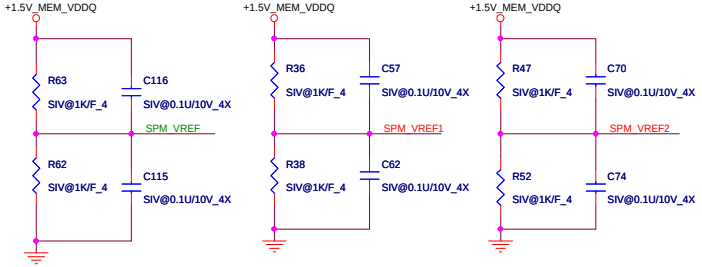

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PROJECT : BL7

Size	Document Number	Rev
	RX881-HT LINK I/F 1/4	D3A

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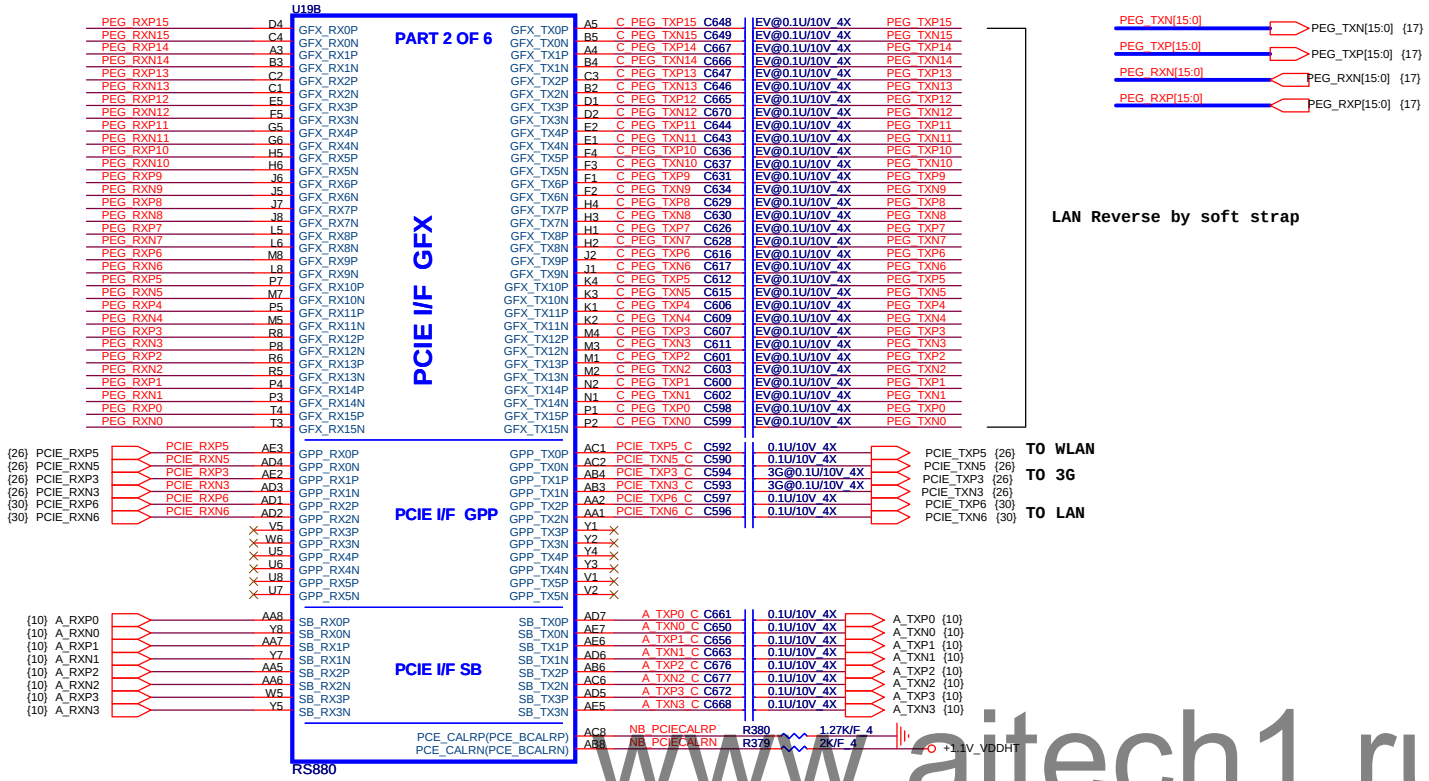

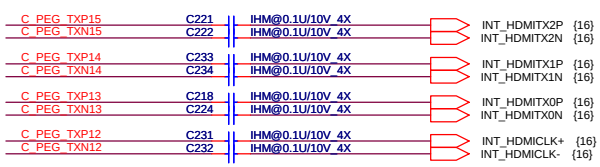

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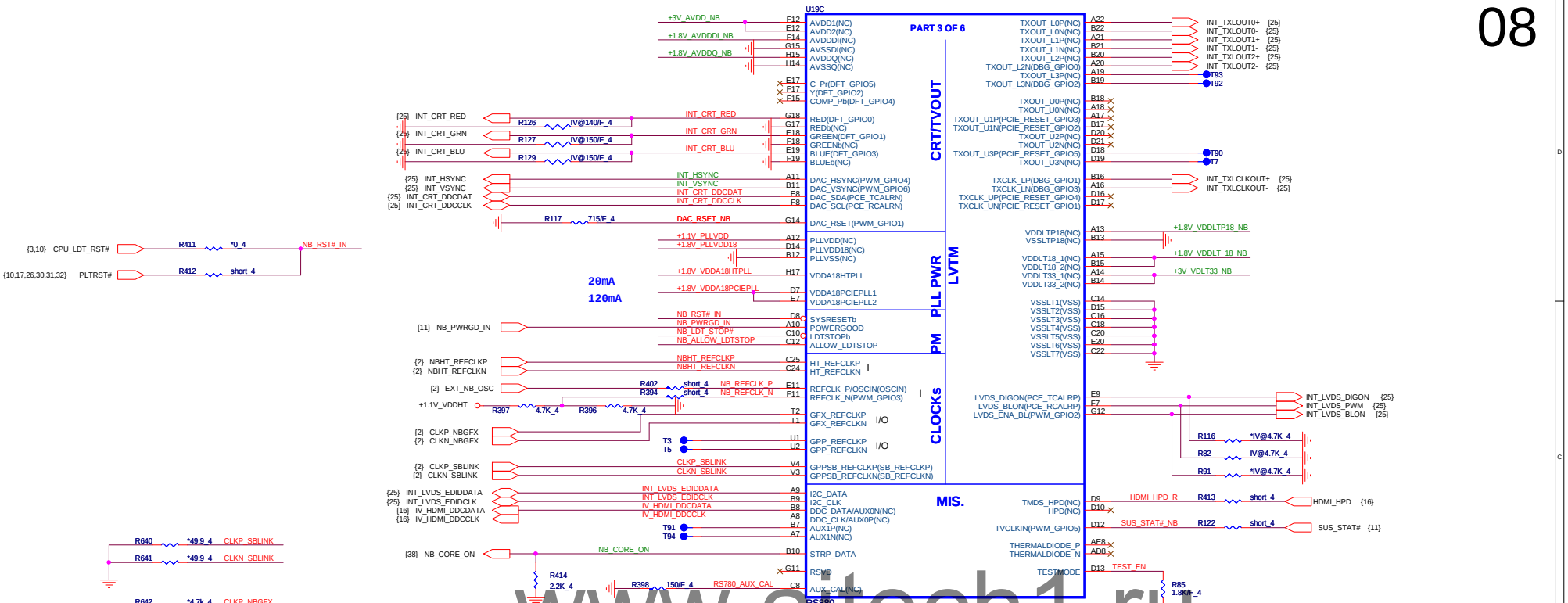
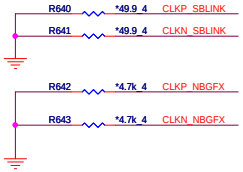
PROJECT : BL7

Size	Document Number	Rev
	RX881-PCIE I/F 2/4	D3A
Date: Friday, March 12, 2010	Sheet 7 of 44	





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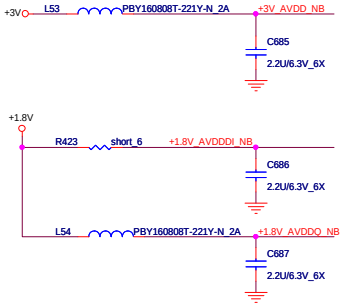
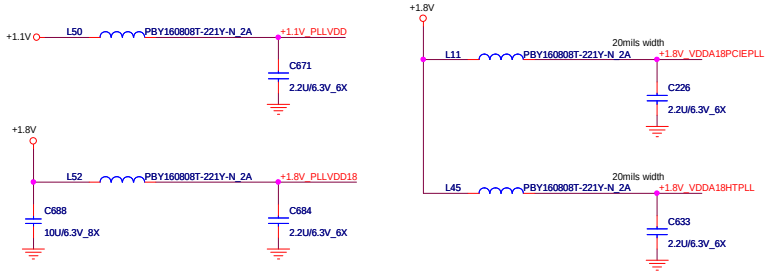
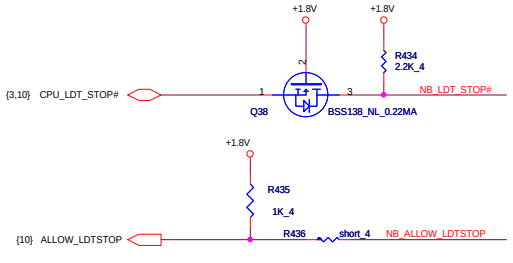
CRT



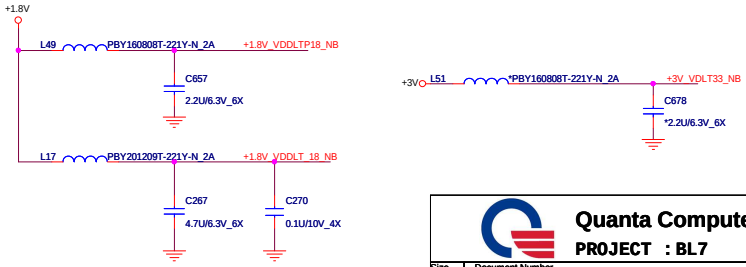
PLL



LDT Level shift



LVDS



RS880M Strapping

Function	Setting
EEPROM Strap 0-->Enable 1-->Disable	R121 *3K/F_4 — R123 3K/F_4 — +3V; SUS_STAT#_NB
Debug Bus 0-->Enable 1-->Disable	R403 *3K/F_4 — R404 3K/F_4 — +3V; INT_VSYNC
Sideport Enable 0-->Enable 1-->Disable	R406 SIV@3K/F_4 — R405 NSIV@4.7K/F_4 — +3V; INT_HSYNC

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PROJECT : BL7

Size	Document Number	Rev
	RX881-SYSTEM I/F 3/4	D3A

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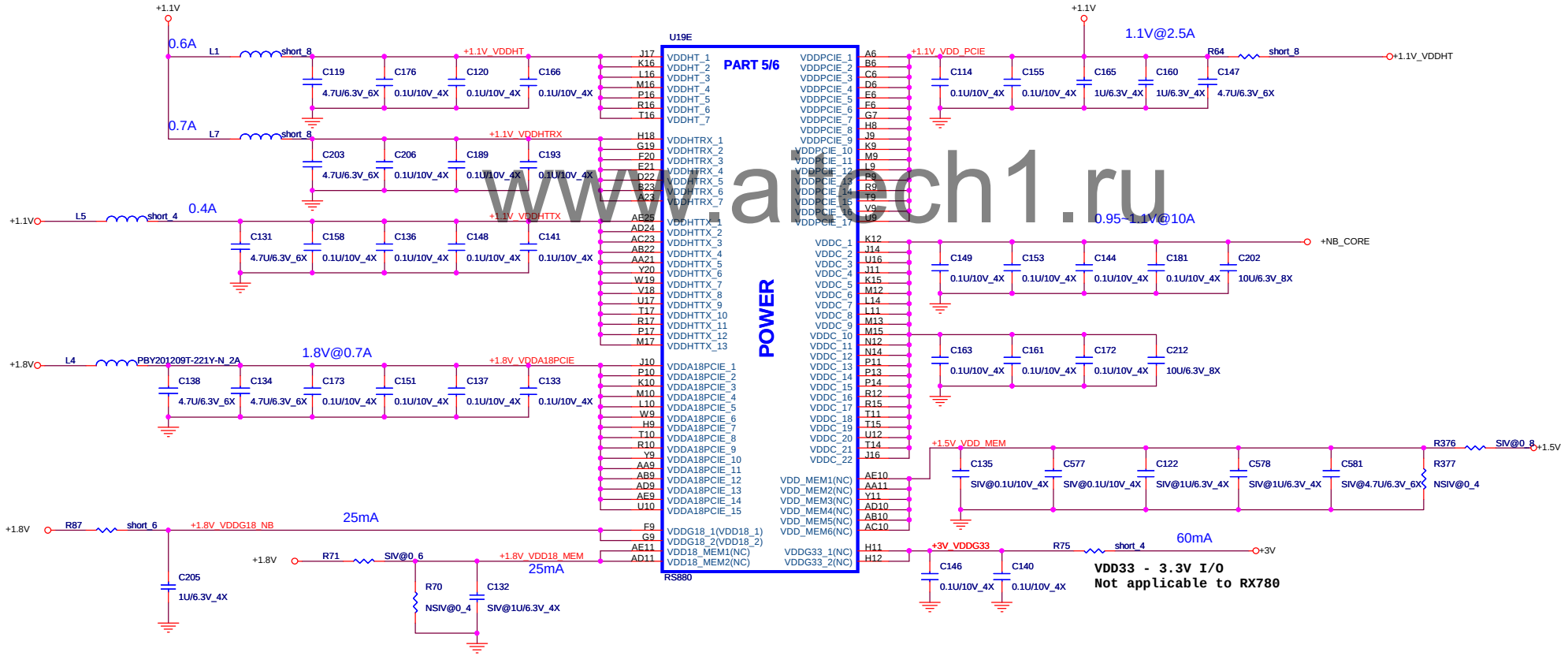
RS880 POWER DIFFERENCE TABLE

PIN NAME	RS880	PIN NAME	RS880
VDDHT	+1.1V	IOPLLVDD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVDD	+1.1V
VDD18_MEM	+1.8V	PLLVDD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDLT18	+1.8V
IOPLLVDD18	+1.8V	VDDLT33	NC



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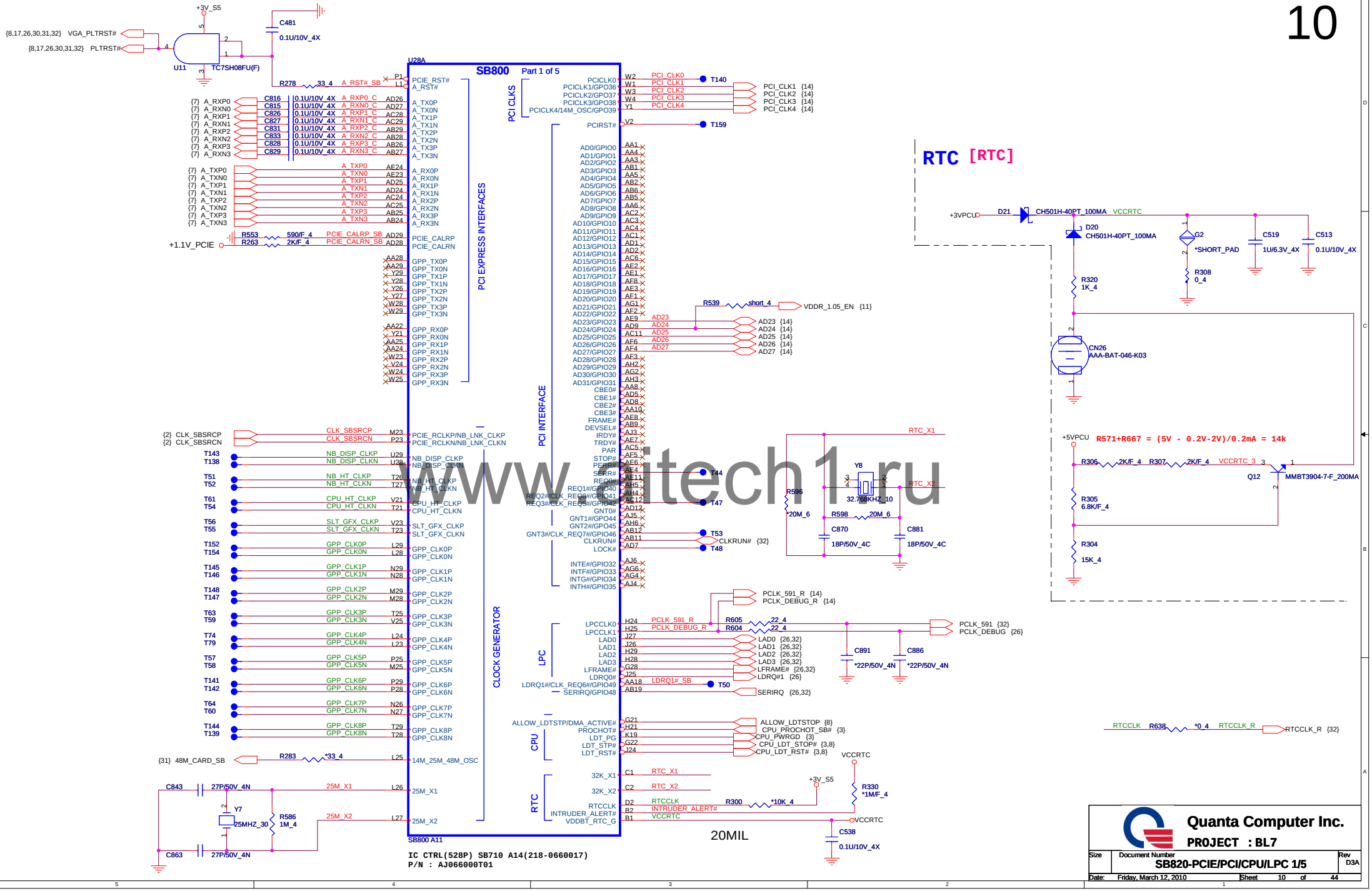
PROJECT : BL7		
Size	Document Number: RX881-POWER5 4/4	Rev: D3A
Date: Friday, March 12, 2010	Sheet 9 of 44	



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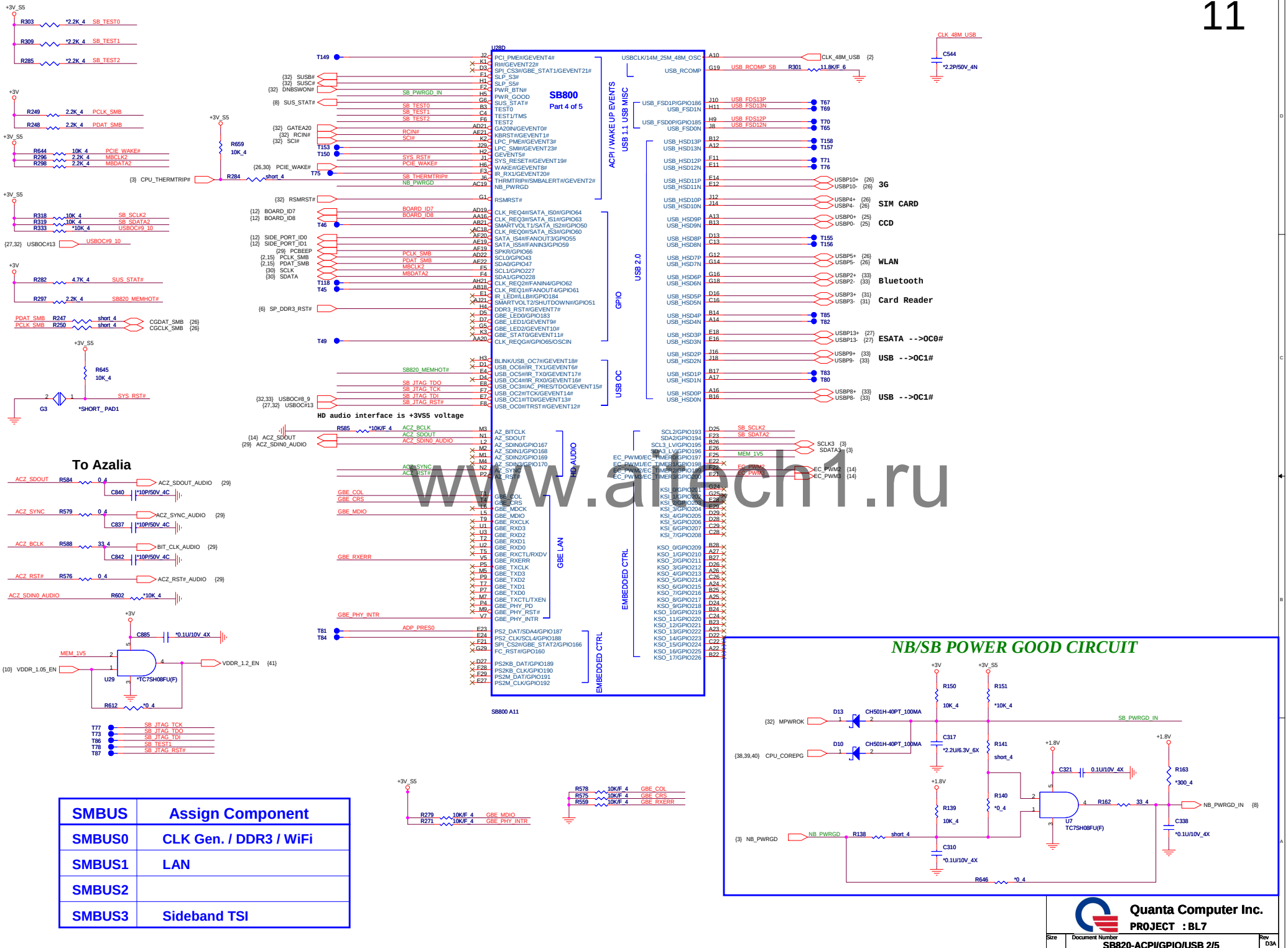

SMBUS	Assign Component
SMBUS0	CLK Gen. / DDR3 / WiFi
SMBUS1	LAN
SMBUS2	
SMBUS3	Sideband TSI

Quanta Computer Inc.
PROJECT : BL7

Size	Document Number	Rev
	SB820-ACPI/GPIO/USB 2/5	D3A

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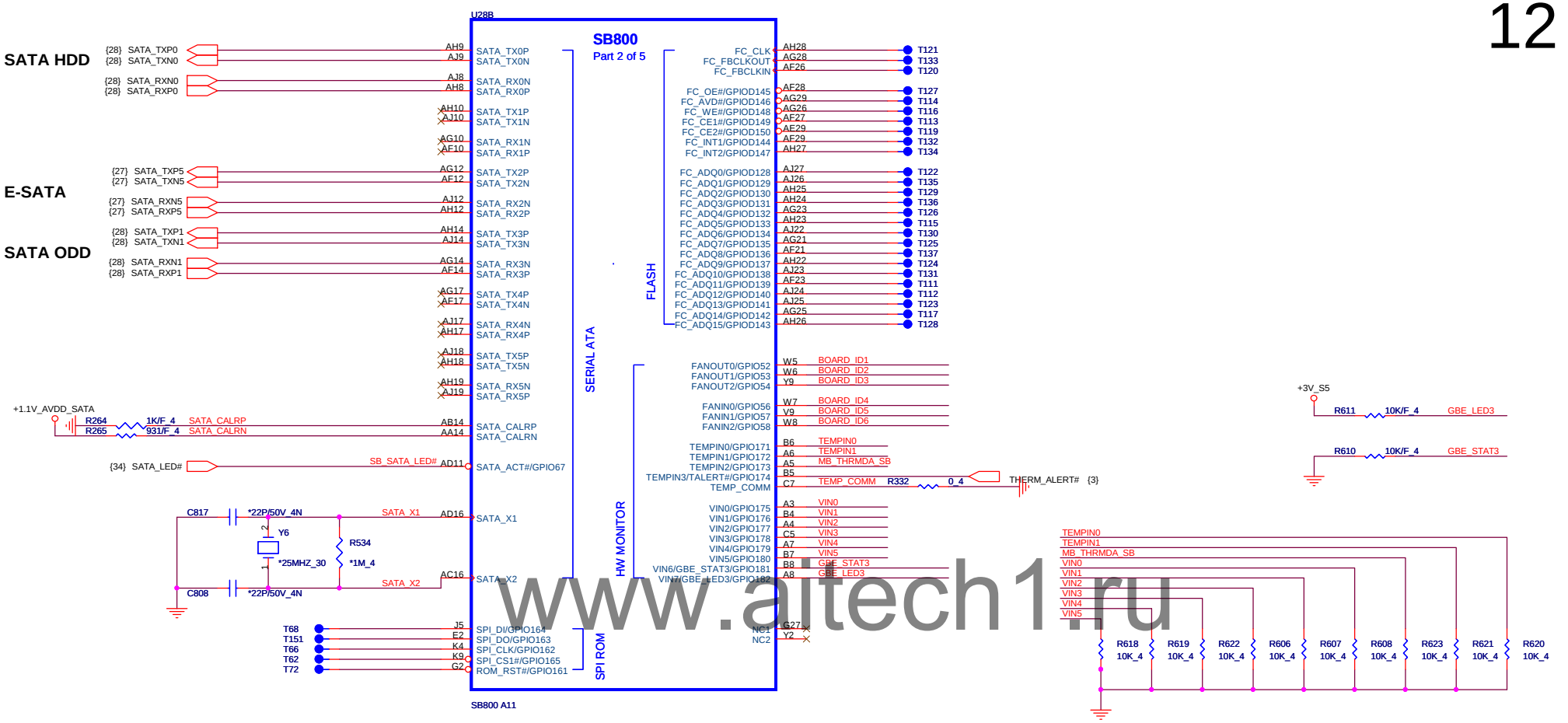

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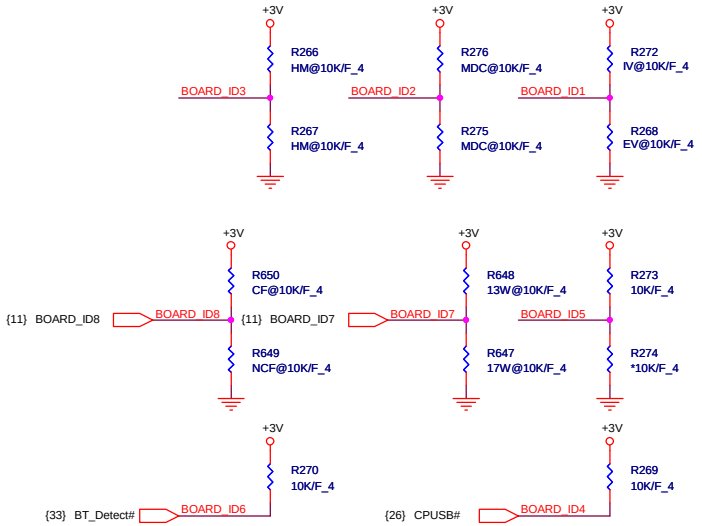
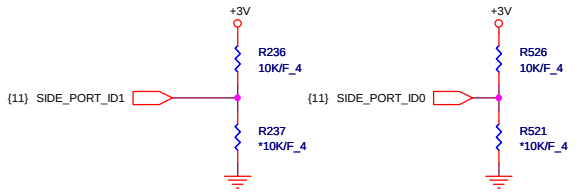
BOARD ID SETTING

Board ID	ID1	ID2	ID3	ID4	ID5	ID6	ID7	ID8
UMA SKU VGA SKU	H L							
W/ MDC W/O MDC		H L						
W/ HDMI W/O HDMI			H L					
W/O 3G W/ 3G				H L				
15" 14"					H L			
W/O BT W/ BT						H L		
13W 17W							H L	
W/ CF W/O CF								H L



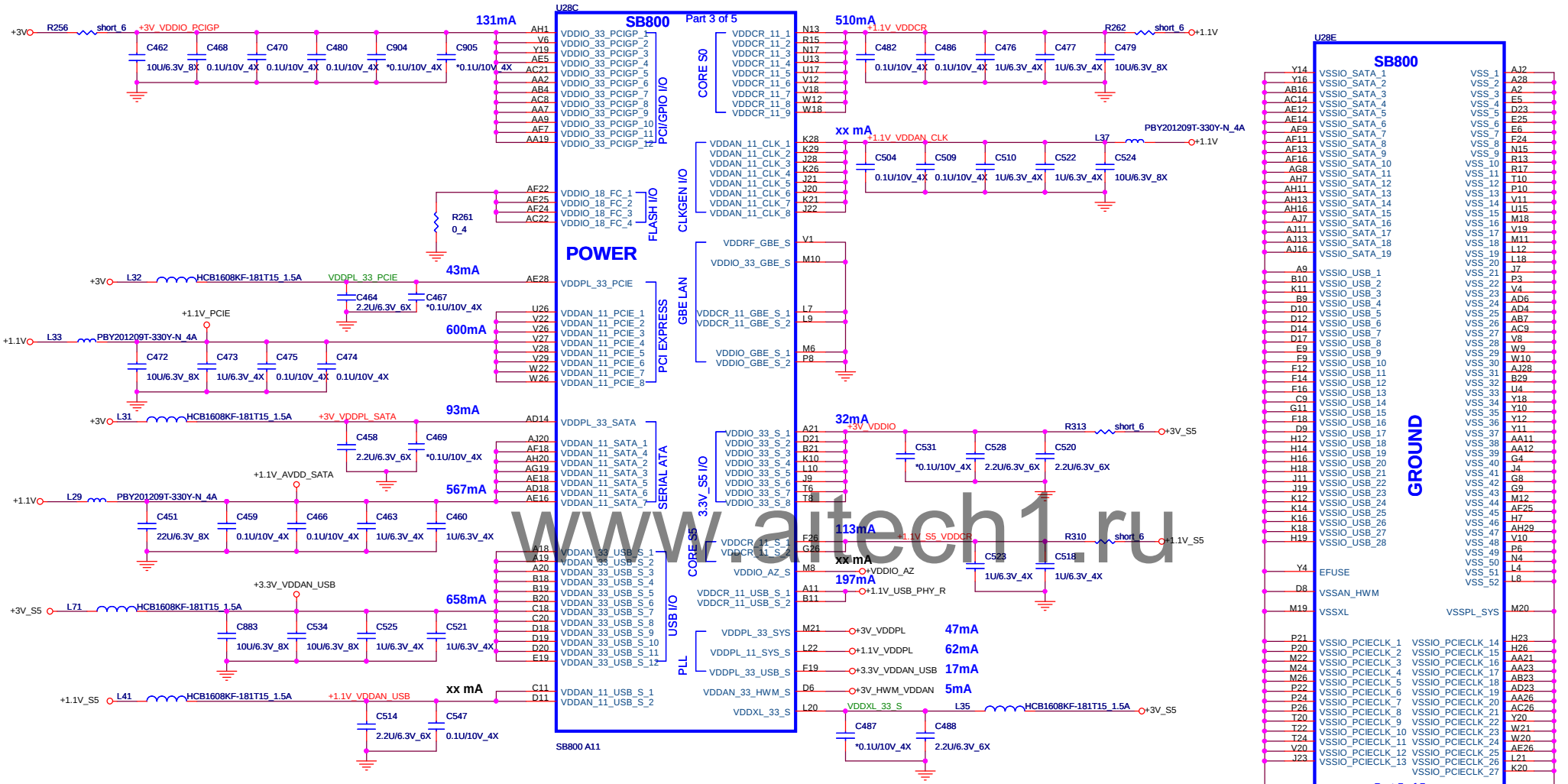


ID1	ID0	Function
0	0	Samsung
0	1	Hynix
1	0	Reserve
1	1	No sideport support

Quanta Computer Inc.
PROJECT : BL7

Size	Document Number	Rev
	SB820-SATA/IDE/HWM/SPI 3/5	D3A

Date: Friday, March 12, 2010 Sheet 12 of 44



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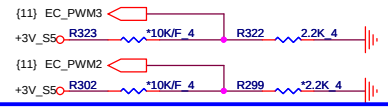
Quanta Computer Inc.
PROJECT : BL7

Size	Document Number	Rev
	SB820-PWR/DECOUPLING 4/5	D3A

Date: Friday, March 12, 2010 Sheet 13 of 44

REQUIRED STRAPS

Ball Name	Strap Name	Default	Description	Setting
LPCCLK0	ECEnableStrap	0	0 -- Disable 1 -- Enable Enable to support enhanced hardware monitor feature	
EC_PWM3 EC_PWM2	ROMTYPE_1 ROMTYPE_0	(0,1)	(0,0) = Firmware Hub (0,1) = LPC (1,0) = SPI (1,1) = Reserved	
LPCCLK1	CLKGEN	0	0 -- External clock 1 -- Integrate clock	
PCICLK1	BIF_GEN2_COMPLIANCE_Strap	1	0 -- PCIE at Gen I mode 1 -- PCIE at Gen II mode	
PCICLK2	BootFailTmeEn	0	0 -- Disable watchdog function 1 -- Enable watchdog function	
PCICLK3	DefaultStrapMode	0	0 -- Disable debug Straps 1 -- Select ext. Debug Straps	
PCICLK4	CPUClksel	1	0 -- Reserved 1 -- Integrated clock mode	
AZ_SDOUT	CoreSpeedMode	0	0 -- Performance mode 1 -- Low Power mode	

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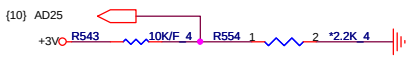
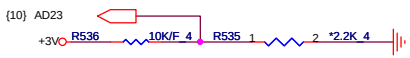
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

Ball Name	Strap Name	Default	Description	Setting
AD27	PciPllByp	1	0 -- ByPass Int PLL 1 -- Int. PLL	
AD26	ILAAutronEnB	1	0 - IAL auto run enable 1 -- IAL auto run disable	
AD25	FCClkByP	1	0 -- Bypass FC Clk 1 -- Int. FC Clk	
AD24	I2CRomEn	1	0 -- Enable EEPROM 1 -- Disable EEPROM	
AD23	PCI_ROM_BOOT	1	0 -- Disable PCI MEM Boot 1 -- Enable PCI MEM Boot	

All signals ihas nternal PU

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PROJECT : BL7

Size	Document Number	Rev
	SB820-STRAPS 5/5	D3A

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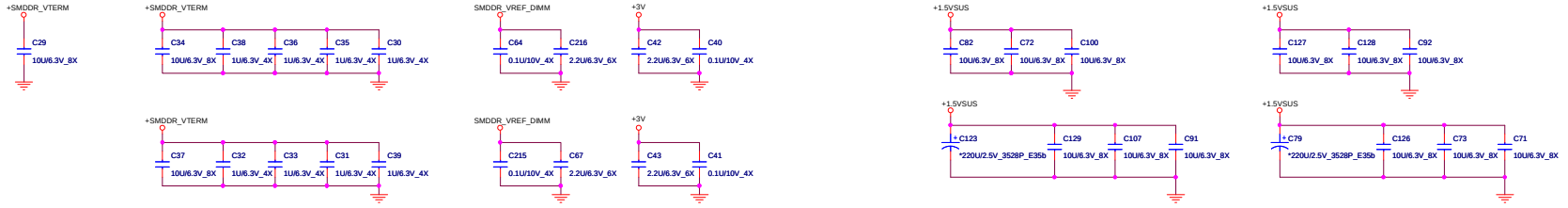
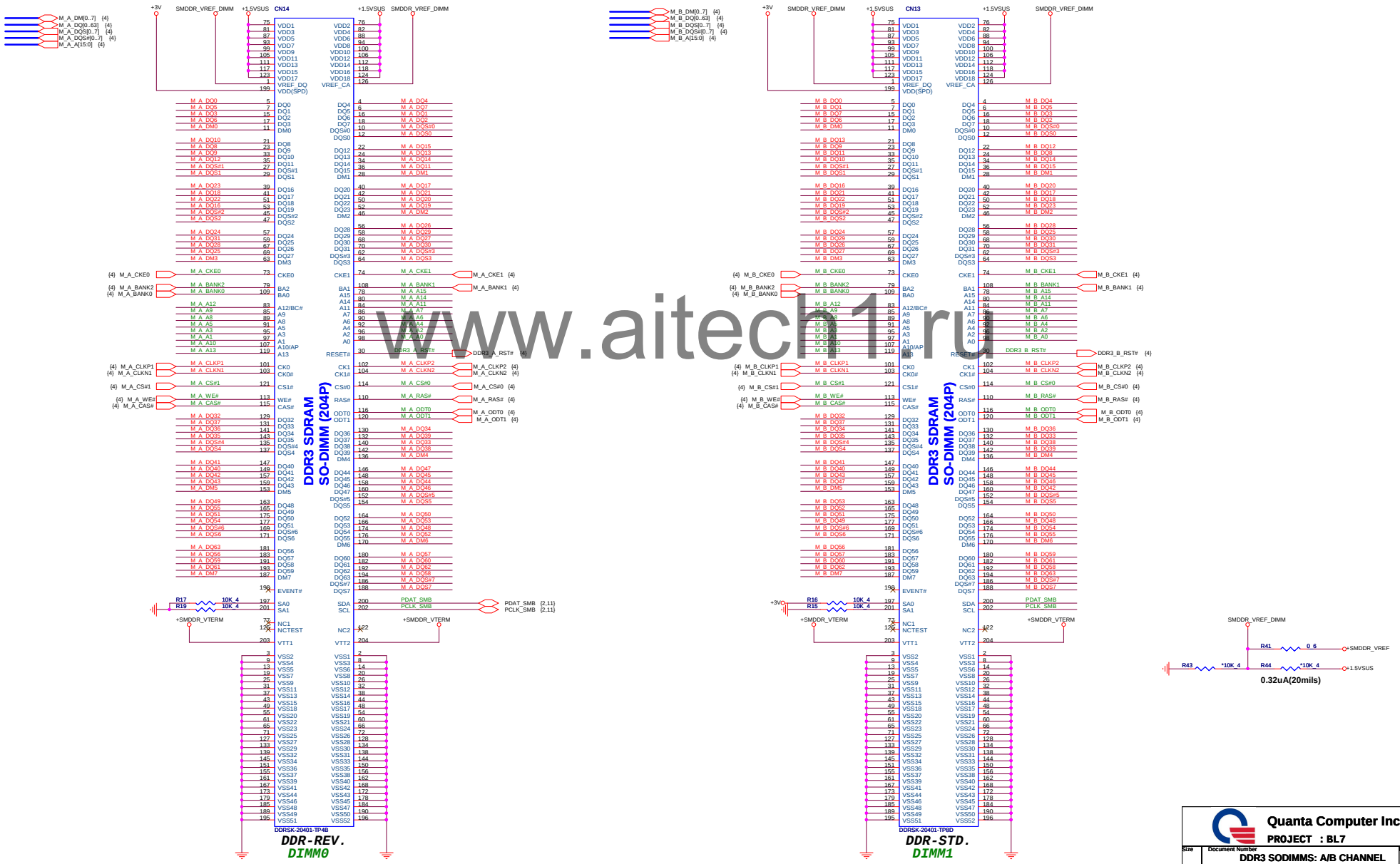
DDRIII

TERMINATOR DECOUPLING CAPACITOR





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Quanta Computer Inc.
PROJECT : BL7
Size | Document Number: DDR3 SODIMMS: A/B CHANNEL | Rev: D3A
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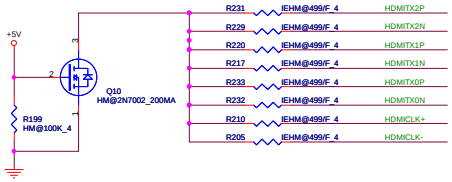
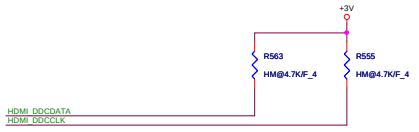
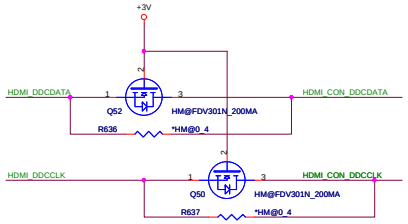
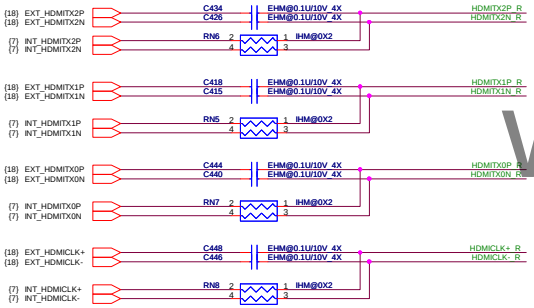


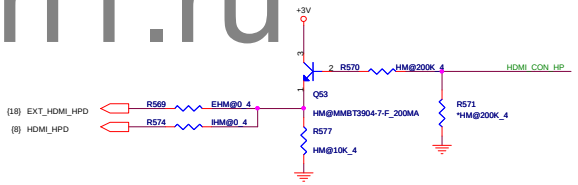


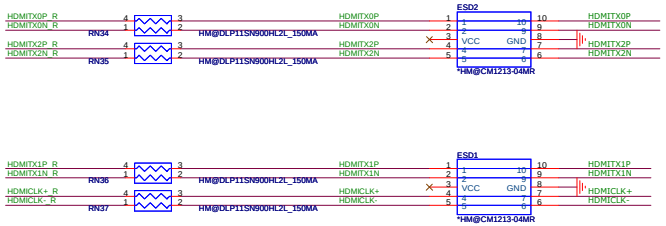


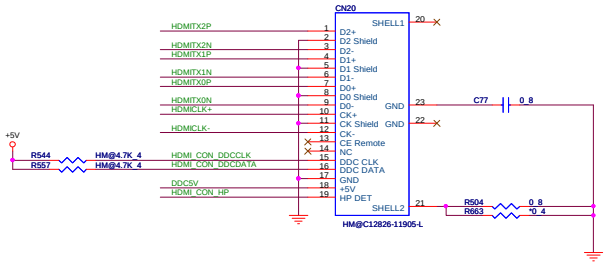
Discrete HDMI

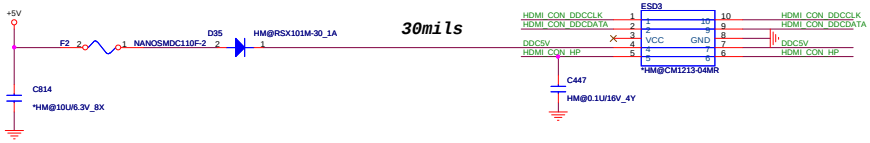


HDMI HPD









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Quanta Computer Inc.
PROJECT : BL7

Size	Document Number	Rev
	HDMI CONN	D3A

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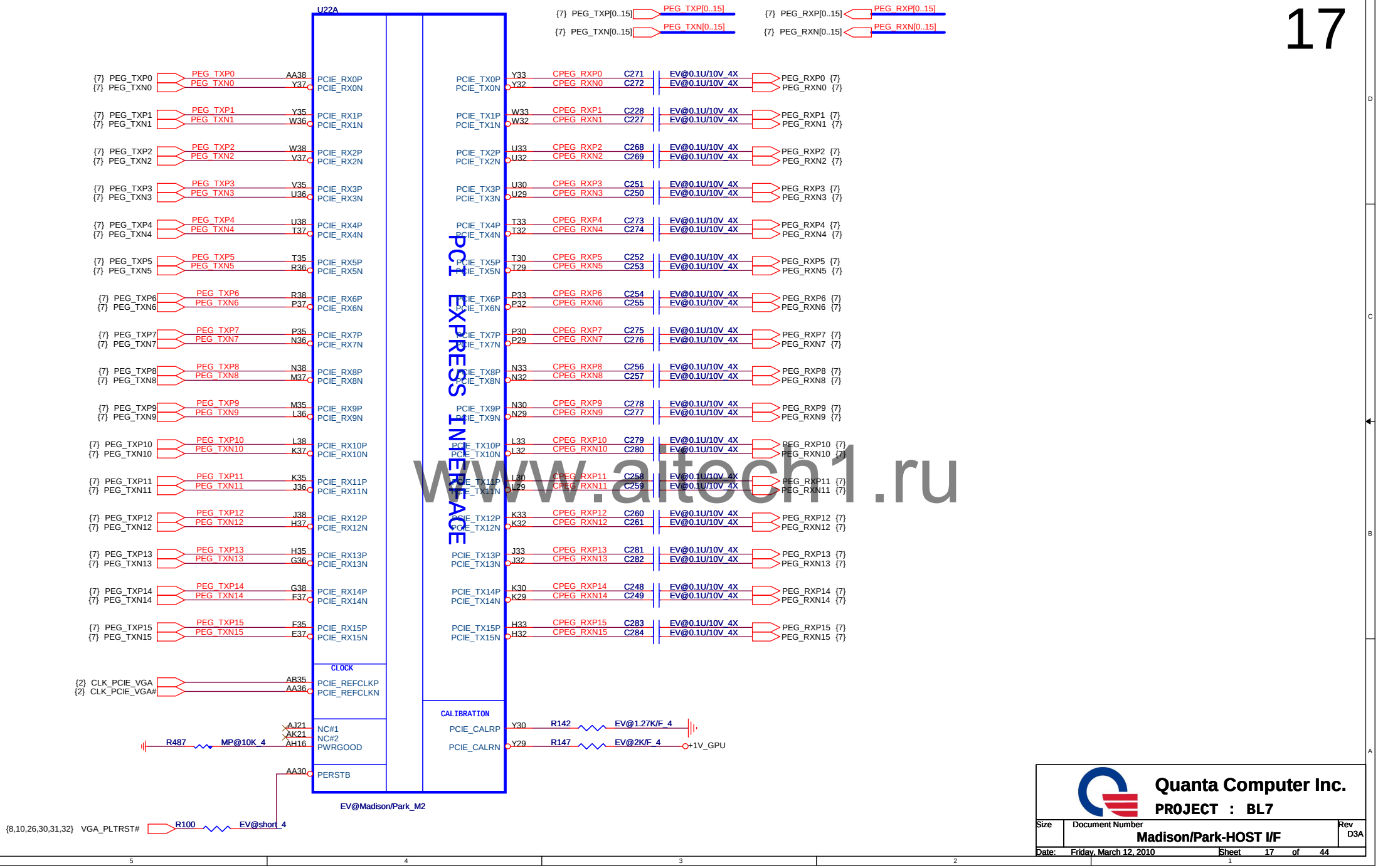

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Quanta Computer Inc.

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	Madison/Park-HOST I/F	D3A

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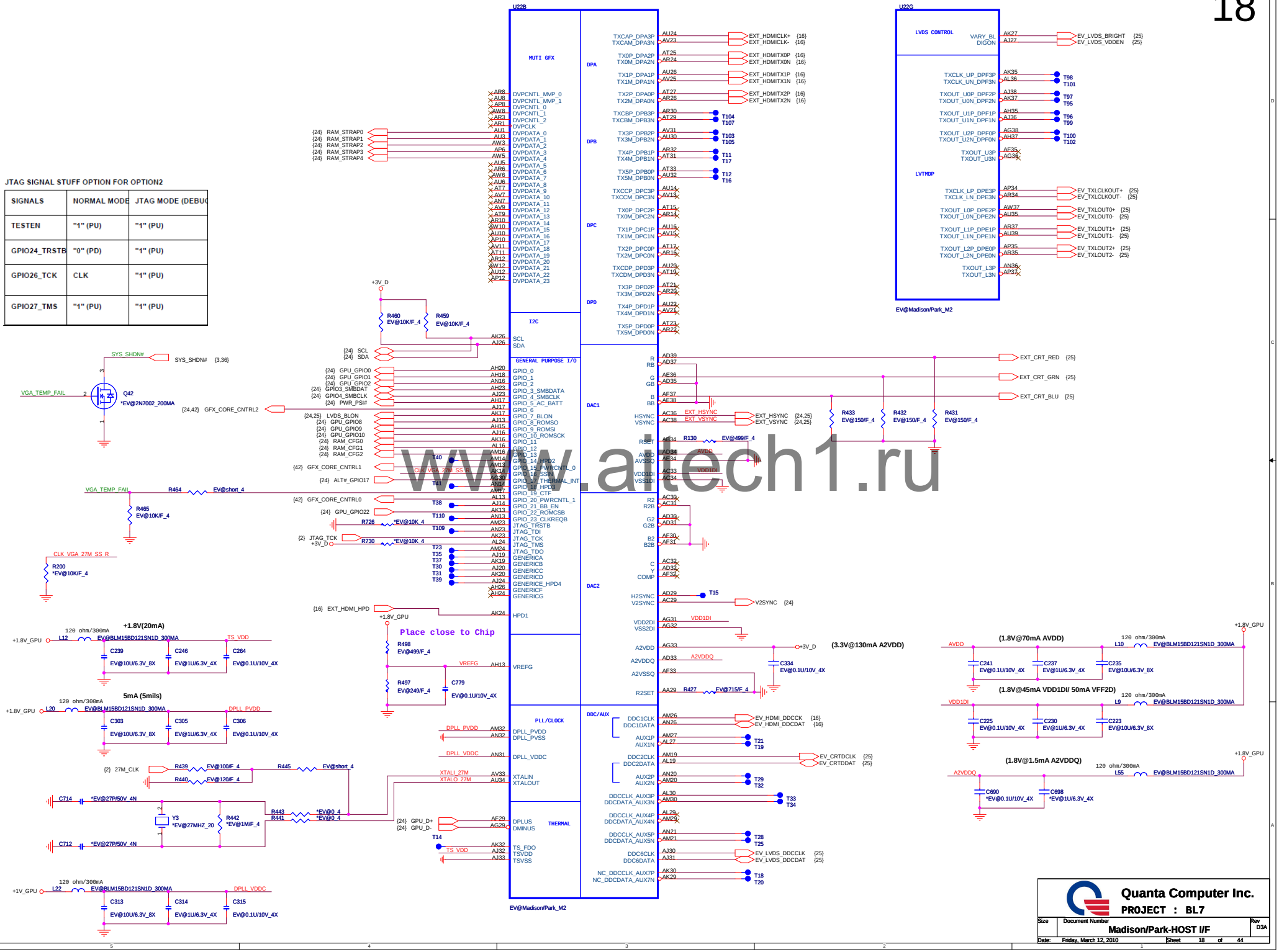
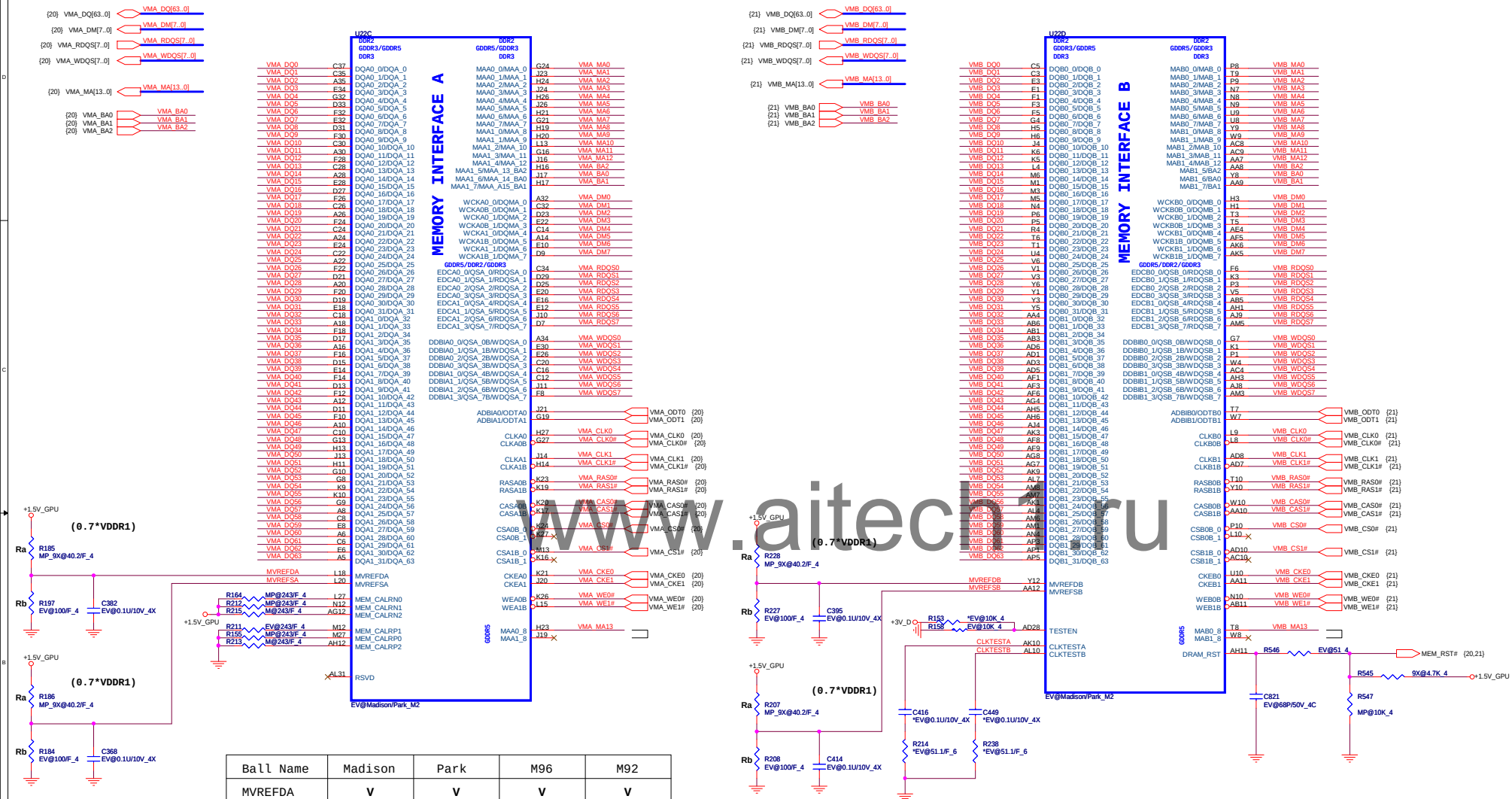
JTAG SIGNAL STUFF OPTION FOR OPTION2

SIGNALS	NORMAL MODE	JTAG MODE (DEBU
TESTEN	"1" (PU)	"1" (PU)
GPIO24_TRSTB	"0" (PD)	"1" (PU)
GPIO26_TCK	CLK	"1" (PU)
GPIO27_TMS	"1" (PU)	"1" (PU)





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Ball Name	Madison	Park	M96	M92
MVREFDA	V	V	V	V
MVREFSA	V	V	V	V
MVREFDB	V	V	V	V
MVREFSB	V	V	V	V
MEM_CALRN0	V	V		
MEM_CALRN1	V	V		
MEM_CALRN2	V			
MEM_CALRP0	V	V		
MEM_CALRP1	V	V	V	V
MEM_CALRP2	V			

DDR3/GDDR3 Memory Stuff Option

	GDDR3	DDR3
MVDDQ	1.8V/1.5	1.5V
Ra	40.2R	40.2R
Rb	100R	100R

	Value	
	MP@	9X@
R185	40.2/F_4	100/F_4
R186	40.2/F_4	100/F_4
R207	40.2/F_4	100/F_4
R228	40.2/F_4	100/F_4

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CHANNEL A: 512MB DDR3 (64M*16*4pcs)

{19} VMA_DQ[63..0] — VMA_DQ[63..0]
{19} VMA_DM[7..0] — VMA_DM[7..0]
{19} VMA_RDQS[7..0] — VMA_RDQS[7..0] — QSA[7..0]
{19} VMA_WDQS[7..0] — VMA_WDQS[7..0] — QSA#[7..0]
{19} VMA_MA[13..0] — VMA_MA[13..0]

TOP Left | BOT Left | BOT Right | TOP Right

Group-A0 VREF

Group-A1 VREF

MEM_A0 CLK

Group-A0 decoupling CAP

Group-A1 decoupling CAP

MEM_A1 CLK

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Quanta Computer Inc.
PROJECT : BL7
Size | Document Number: VRAM_A: DDR3-64M*16*4PCS | Rev: D3A
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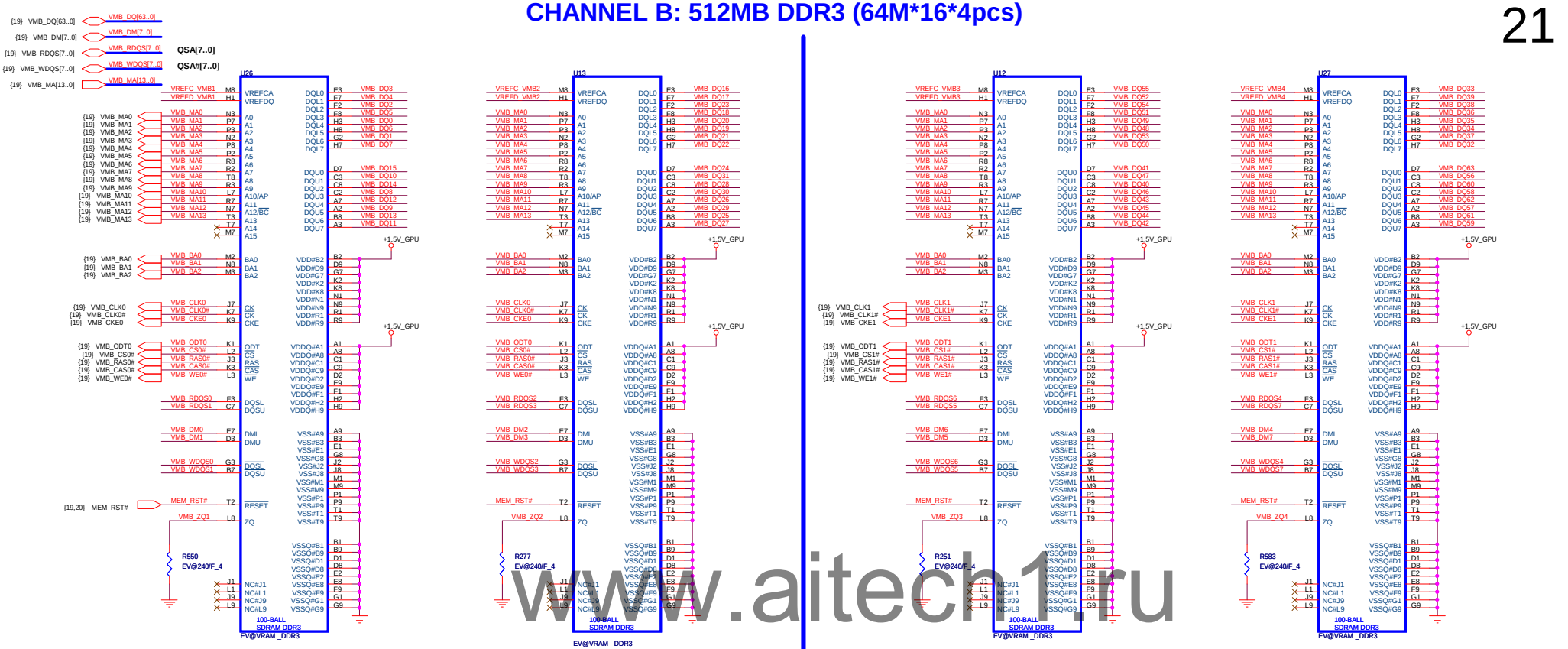
CHANNEL B: 512MB DDR3 (64M*16*4pcs)



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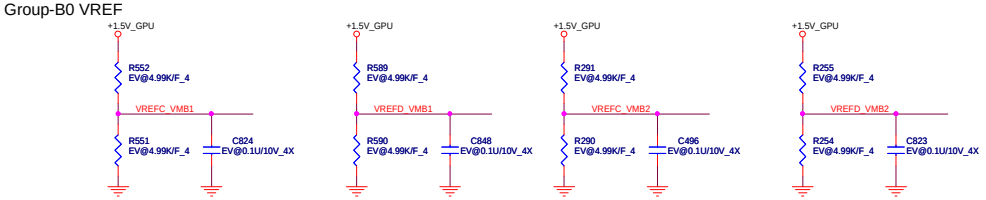
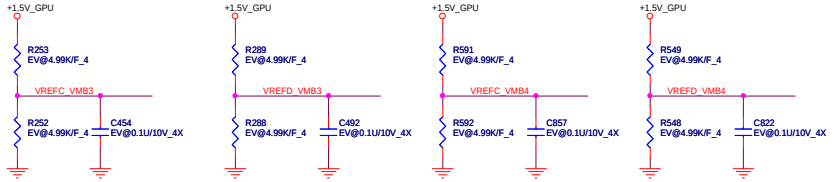
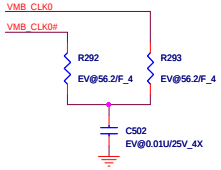
Group-B0 VREF



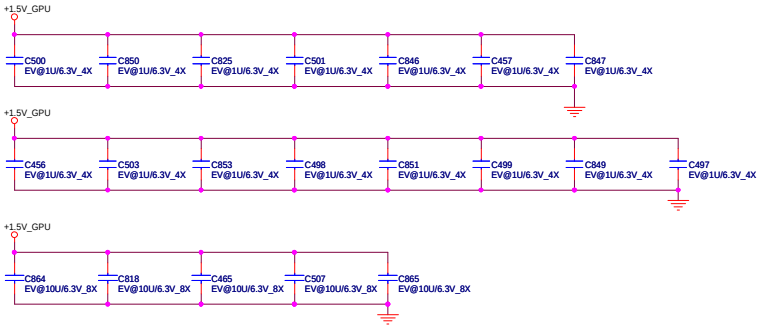
Group-B1 VREF



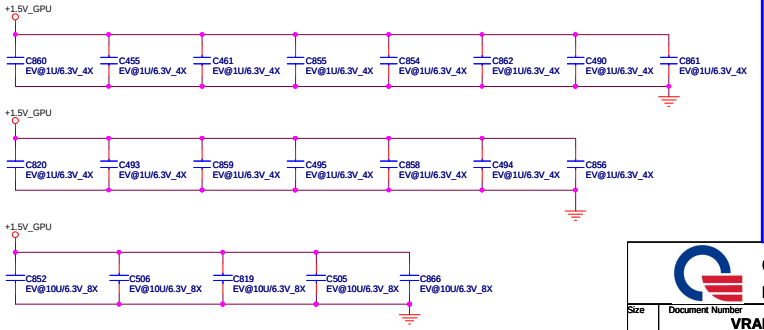
MEM_B0 CLK



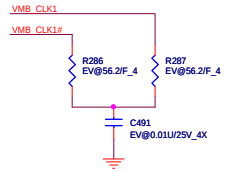
Group-B0 decoupling CAP



Group-B1 decoupling CAP



MEM_B1 CLK



Quanta Computer Inc.
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Size	Document Number	Rev
	VRAM_B: DDR3-64M*16*4PCS	D3A
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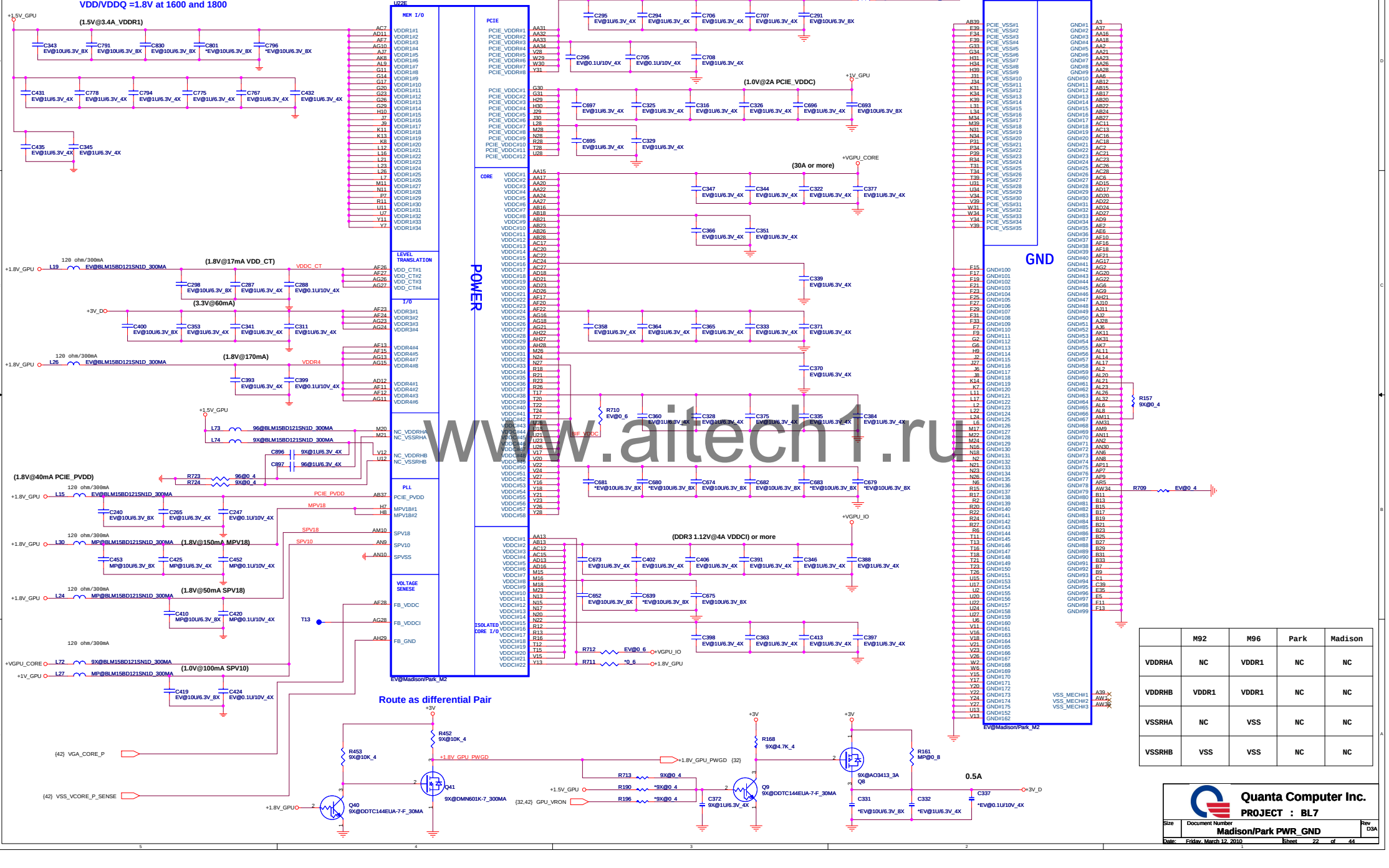
For Madison and Park VDDCI and VDDC can share one common regulator

VDD/VDDQ =1.5V at 1333
VDD/VDDQ =1.8V at 1600 and 1800



	M92	M96	Park	Madison
VDDRHA	NC	VDDR1	NC	NC
VDDRHB	VDDR1	VDDR1	NC	NC
VSSRHA	NC	VSS	NC	NC
VSSRHB	VSS	VSS	NC	NC

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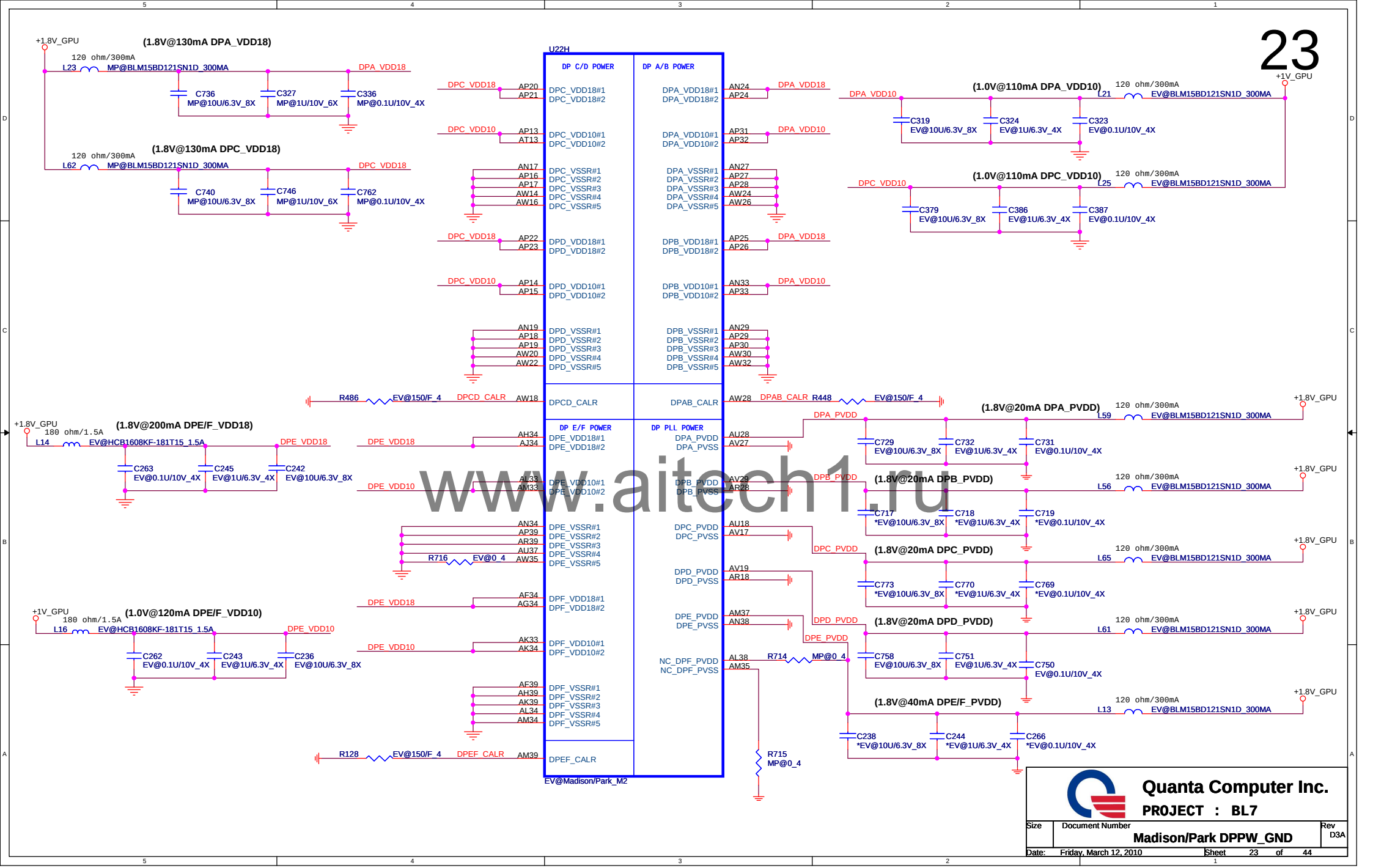

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Quanta Computer Inc.		
PROJECT : BL7		
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	Madison/Park DPPW_GND	D3A
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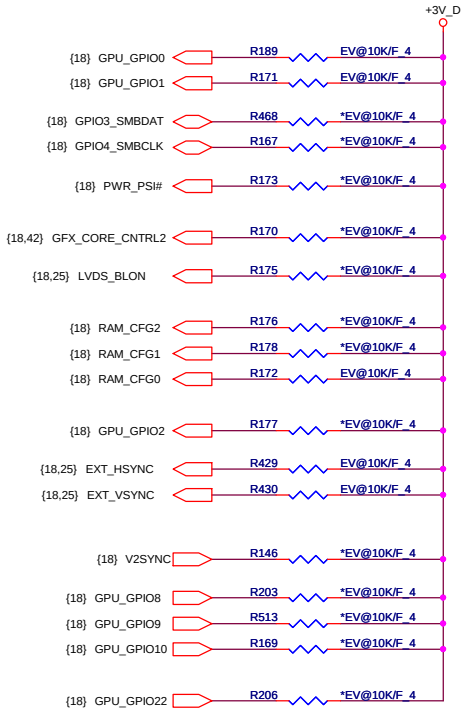
PIN STRAPS



Memory Aperture size	
RAM_CFG[2:0]	Size
000	128MB
001	256MB
010	64MB
011	32MB

ROM Table		
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	1	Both DP & HDMI

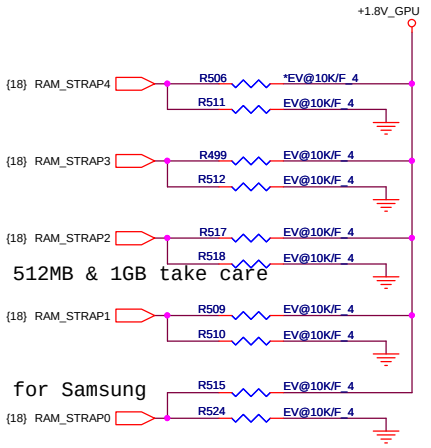
CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

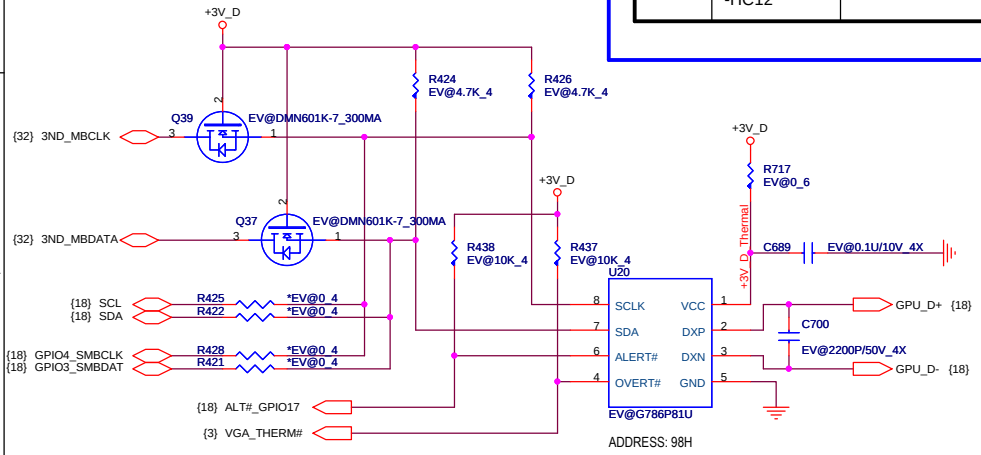
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM (Only for GDDR5) 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT NUMONYX M25P10A : 101	000	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA VIP: Video Capture Port Interface	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

DDR3 Memory TYPE

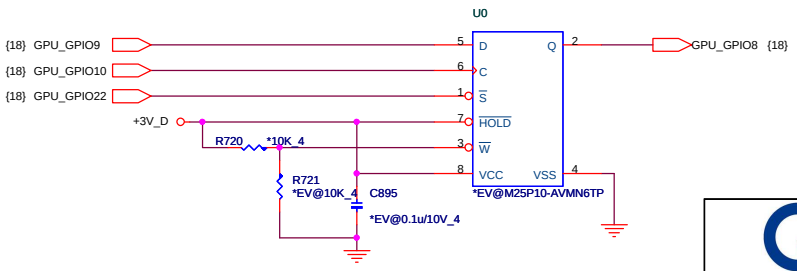
Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP3 DVPDATA_3	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0	RAM_STRAP4 15"	RAM_STRAP4 14"
Hynix	H5TQ1G63BFR -12C	AKD5LZGTW00 (64M*16)	512MB	0	1	0	0	0	1
			1GB	0	0	0	0	0	1
			2GB	0	0	1	0	0	1
Samsung	K4W1G1646E -HC12	AKD5LGGT502 (64M*16)	512MB	0	1	0	1	0	1
			1GB	0	0	0	1	0	1
	K4W2G1646B -HC12	AKD5MGGT501	2GB	0	0	1	1	0	1



Thermal Sensor



EEPROM



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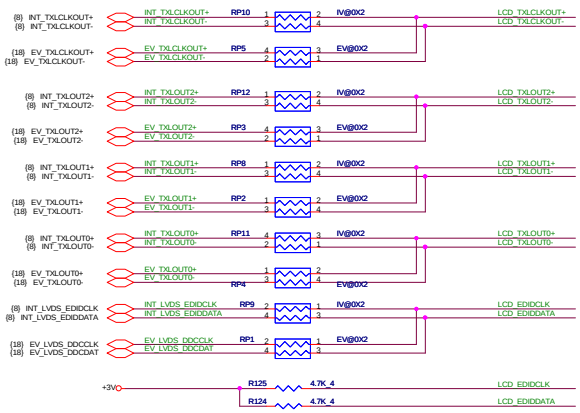
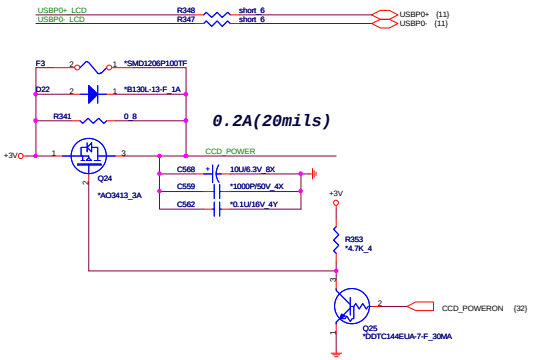
LVDS Signals

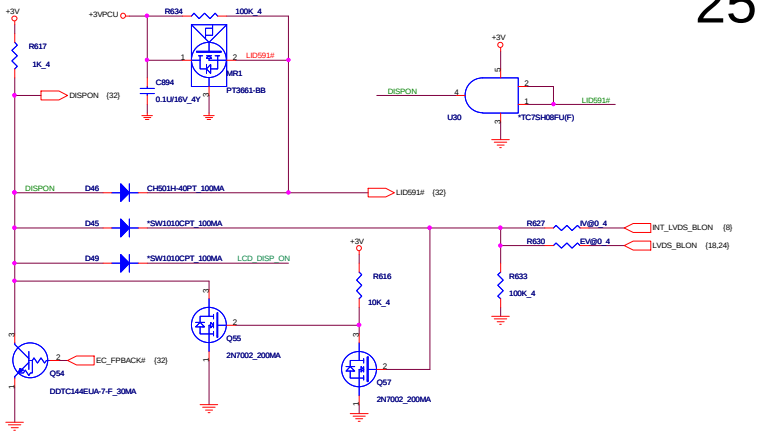


LVDS Enable

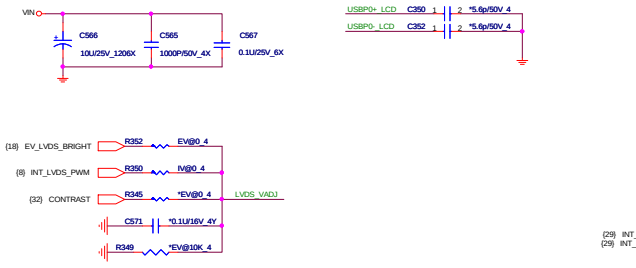
CCD

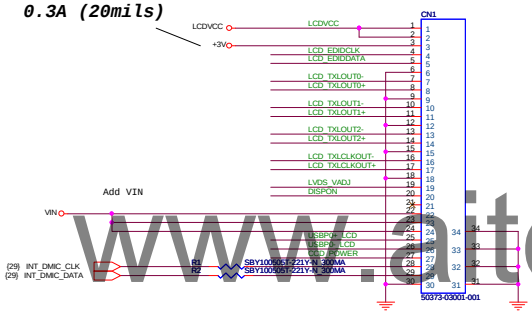


HALL SENSOR&BACK LIGHT SWITCH

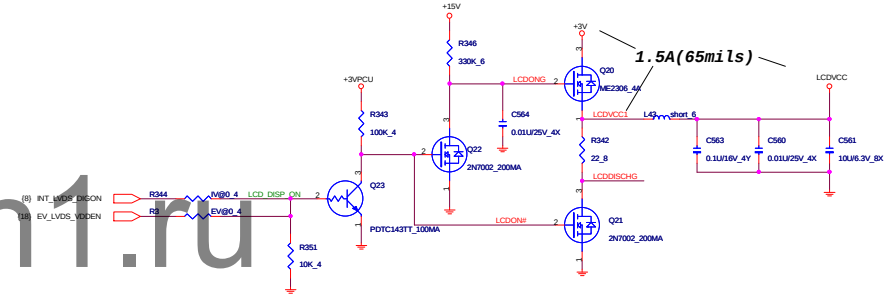


LCD Panel Module

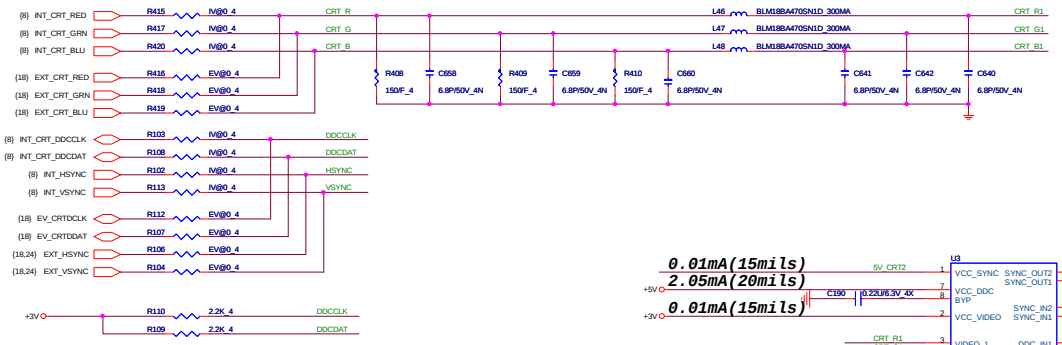


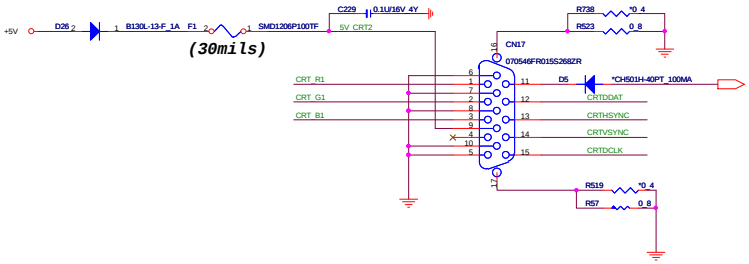


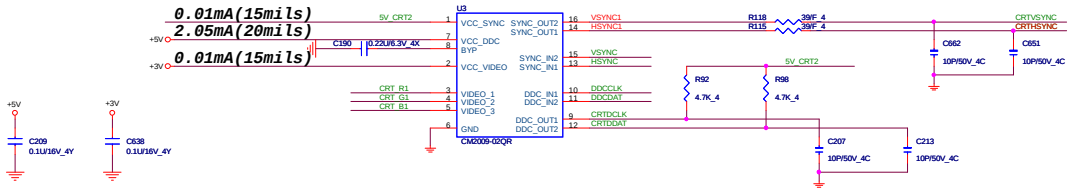
LCD POWER SWITCH



CRT







Quanta Computer Inc.		
PROJECT : BL7		
Size	Document Number: LCD/LED Panel/CCD	Rev: D3A
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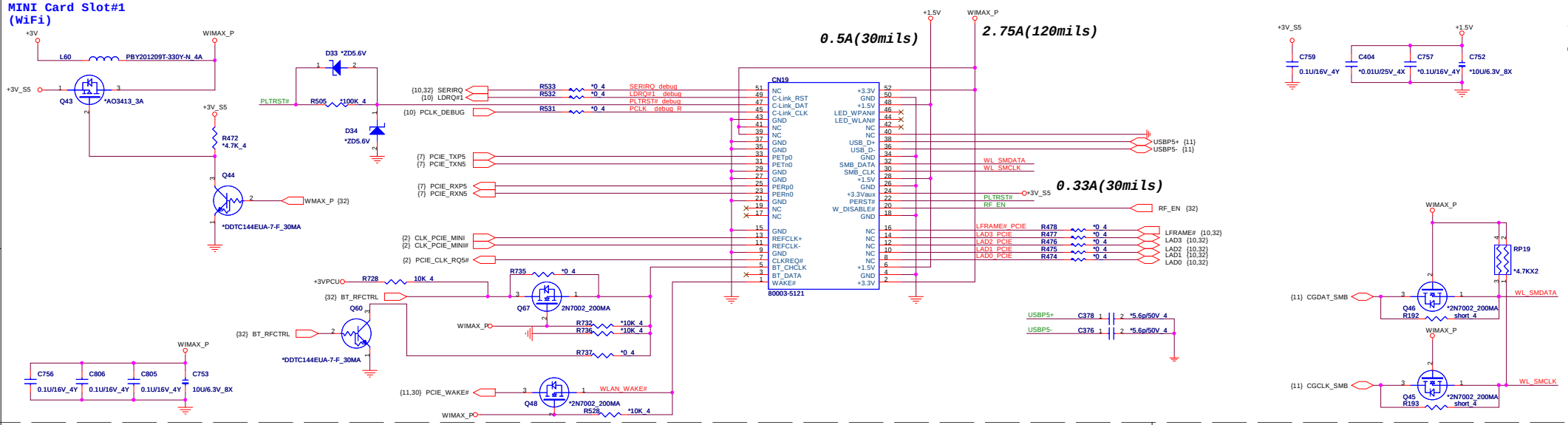
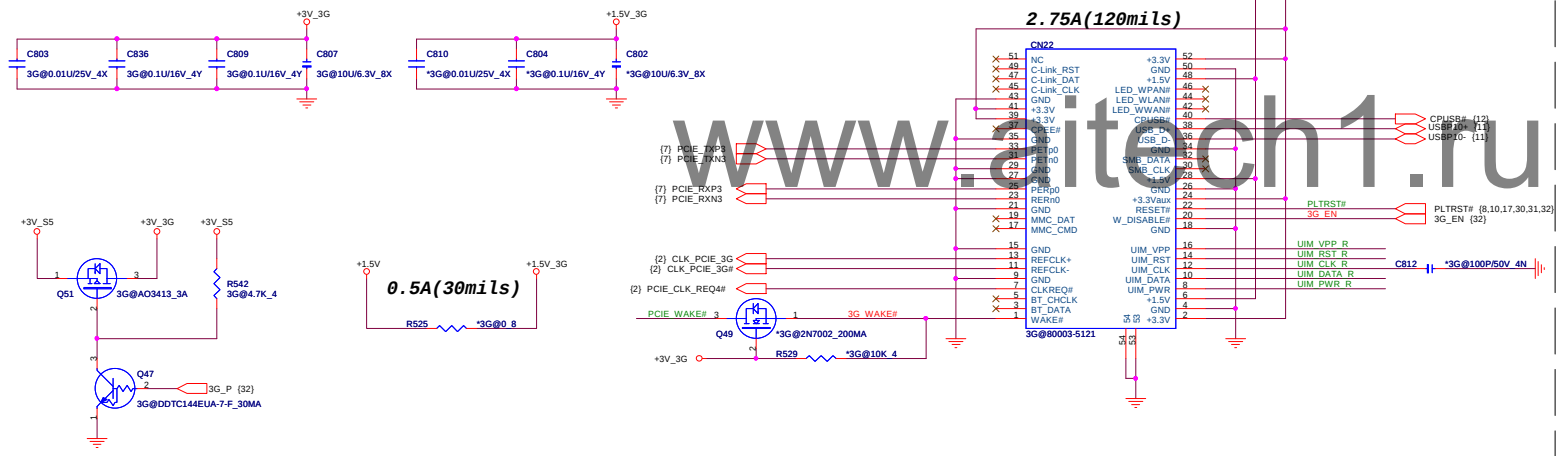
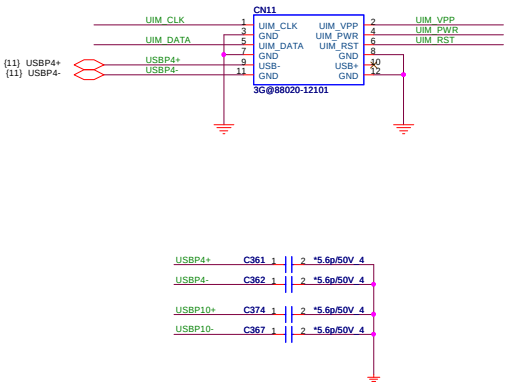
MINI Card Slot#1 (WiFi)



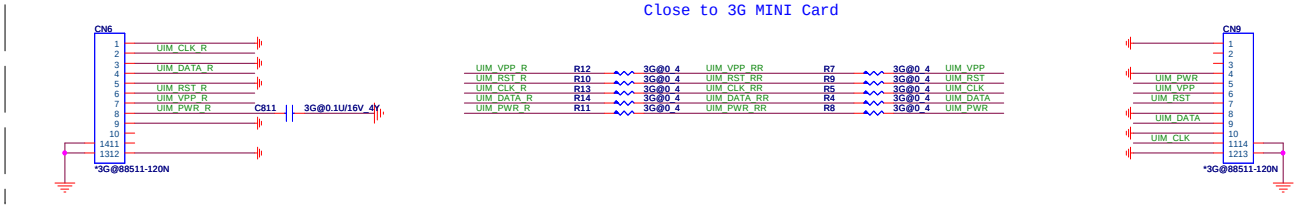
MINI Card Slot#2 3G



SIM CARD board to board



3G CONN



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Quanta Computer Inc.
PROJECT : BL7
Size | Document Number: MINI CARD(WLAN/3G/SIM Card) | Rev: D3A
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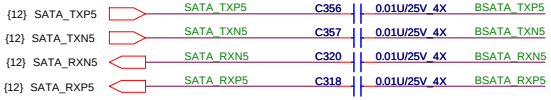
ESATA Re-driver IC



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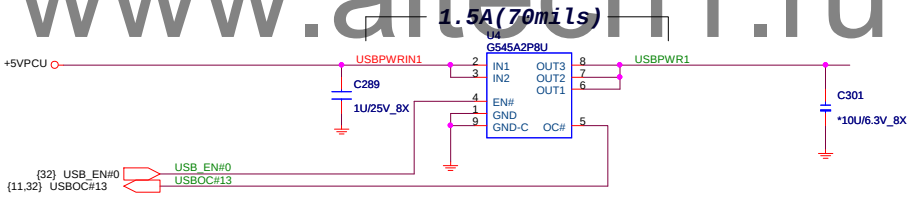
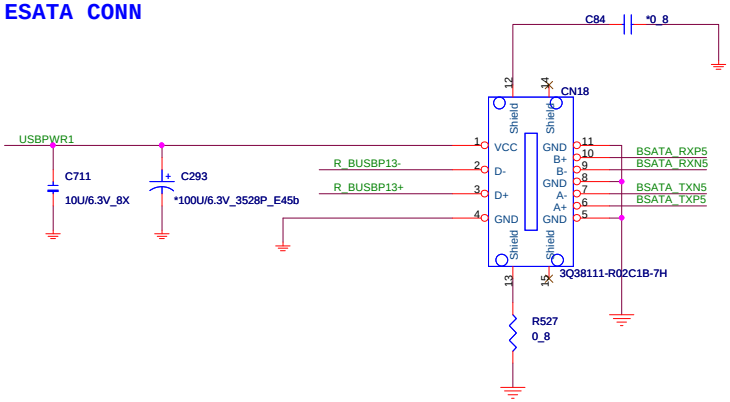
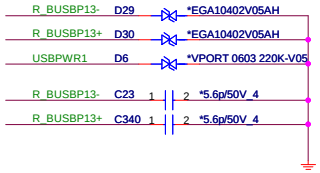
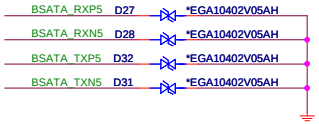


ESATA CONN







Quanta Computer Inc.

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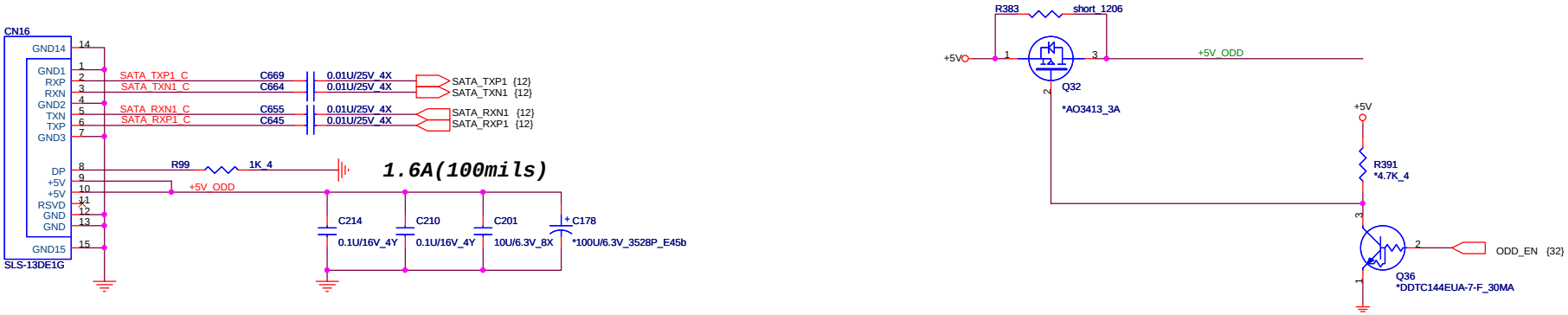
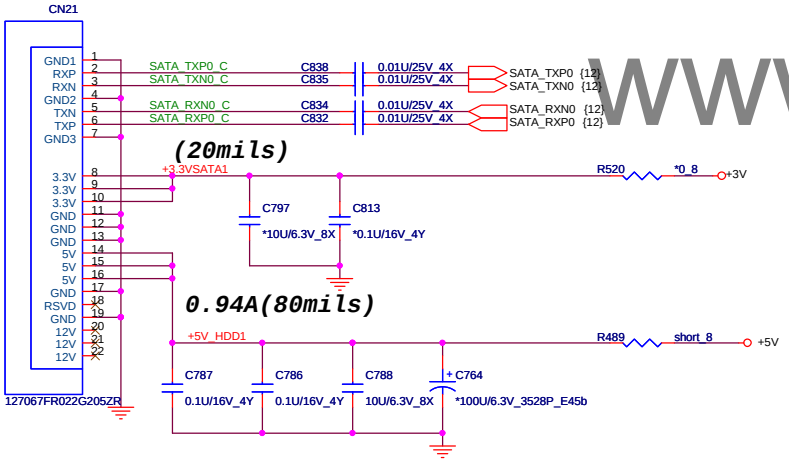
SATA ODD

[ODD]



SATA HDD

[HDD]



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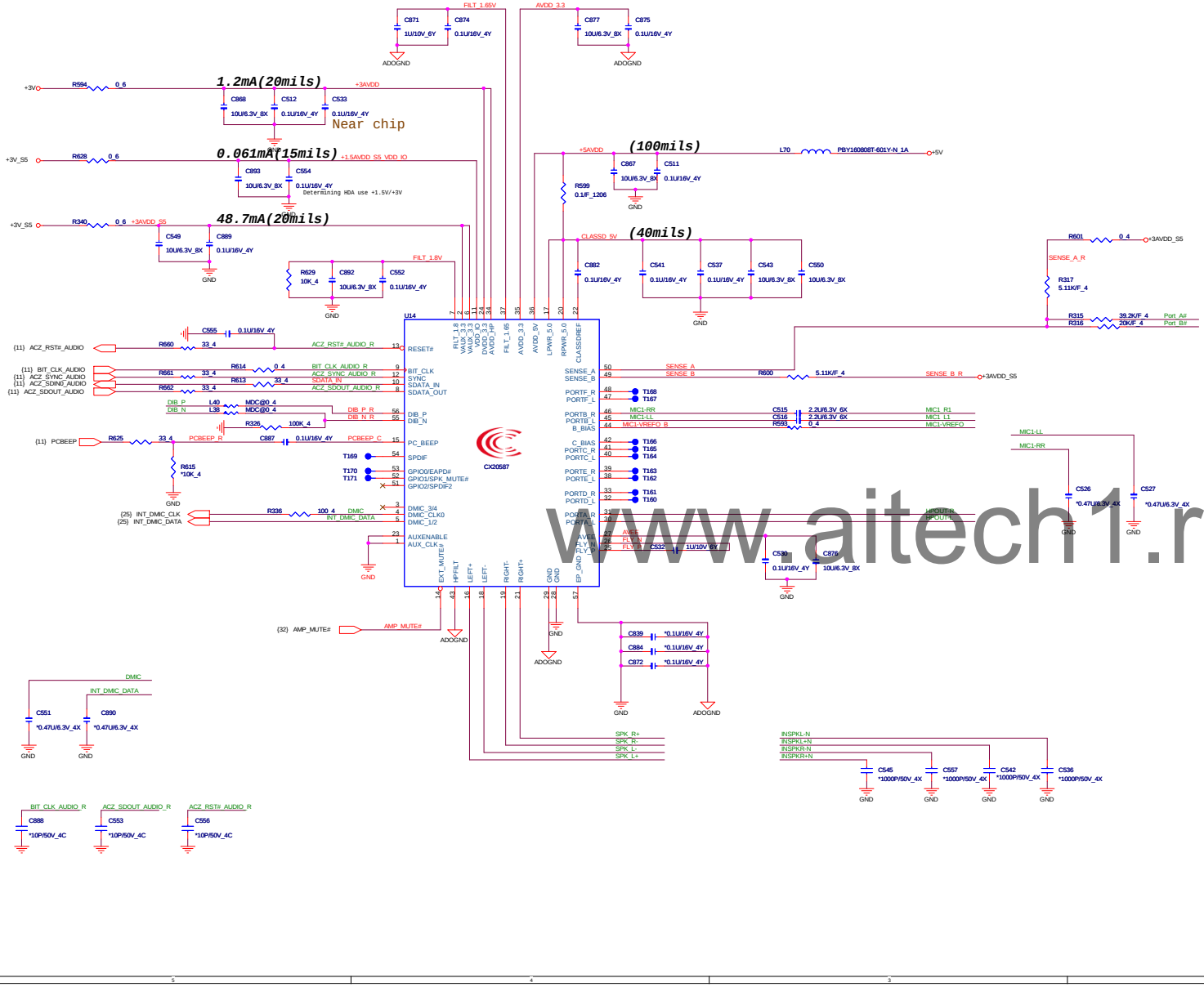
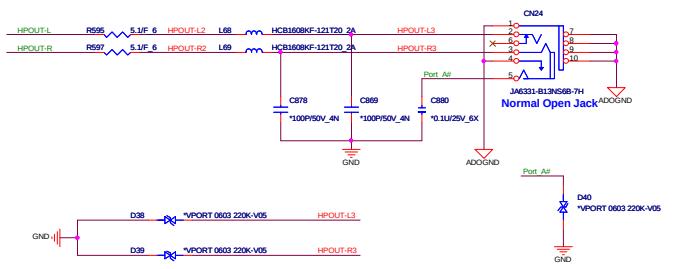
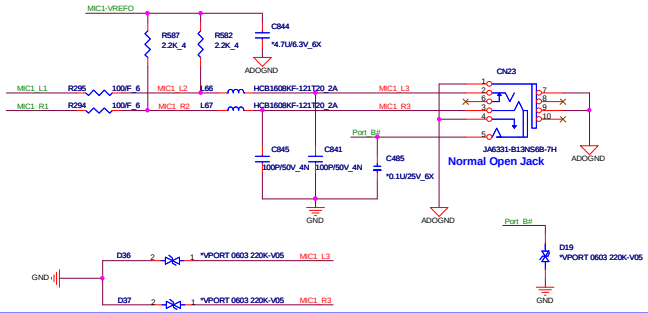
Codec (CX20587)



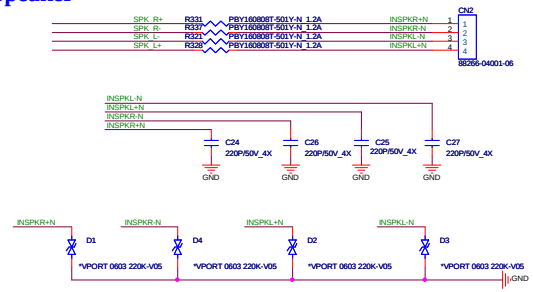
Earphone



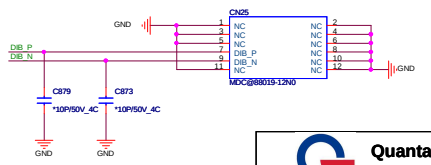
External MIC



Internal Speaker



MDC



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	Audio Codec (CX20583)	03A
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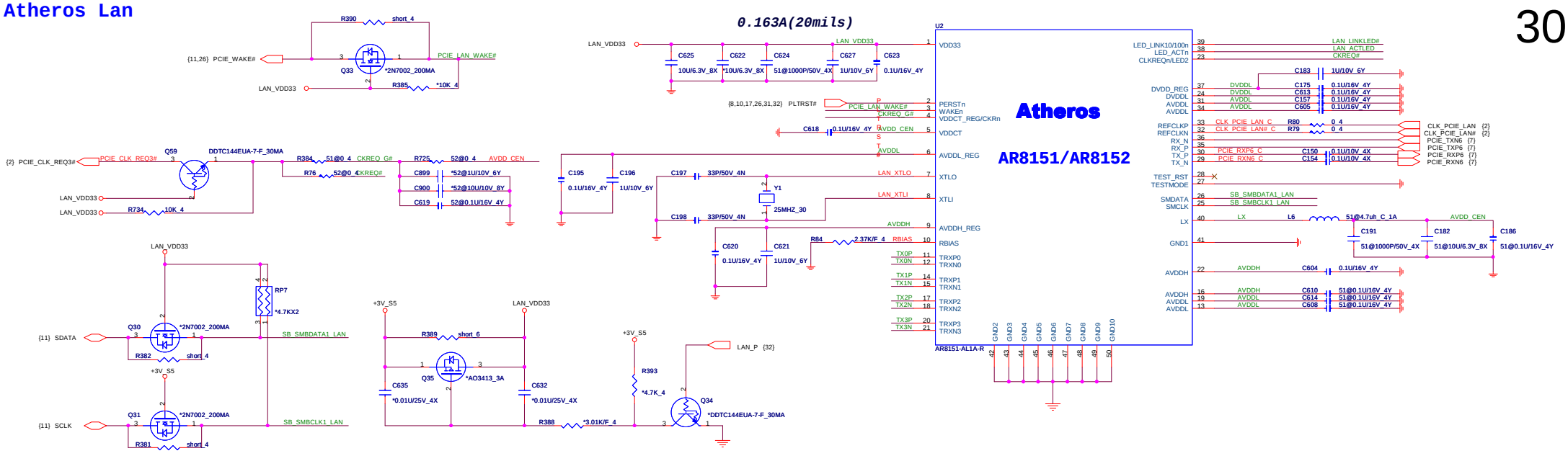
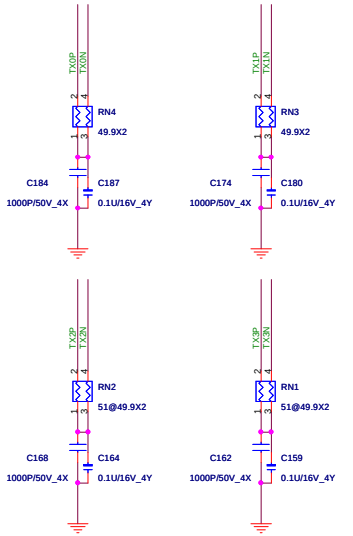
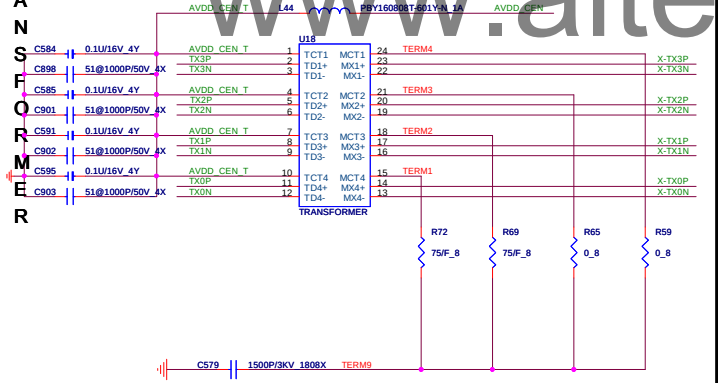
Atheros Lan



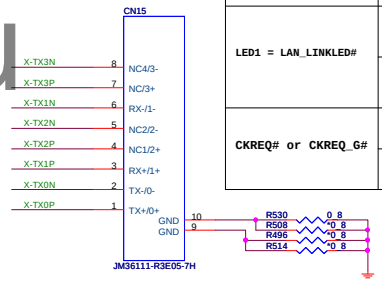
PLACE NEAR LAN IC SIDE



TRANSFORMER



RJ45



LED0 = LAN_ACTLED	1	Over-clocking enable (default = 1)
	0	Over-clocking disable
LED1 = LAN_LINKLED#	1	SWR switch-mode regulator select Giga LAN pull High (default = 1)
	0	LDO linear regulator select 10/100M LAN pull Low
CKREQ# or CKREQ_G#	1	Normal function
	0	ATE test mode

LAN_ACTLED C83 *470P/50V_4X
LAN_LINKLED# C170 *470P/50V_4X

LAN_ACTLED R635 5.1K/F_6
LAN_VDD33 R53 51@5.1K/F_6 LAN_LINKLED# R729 52@5.1K/F_6

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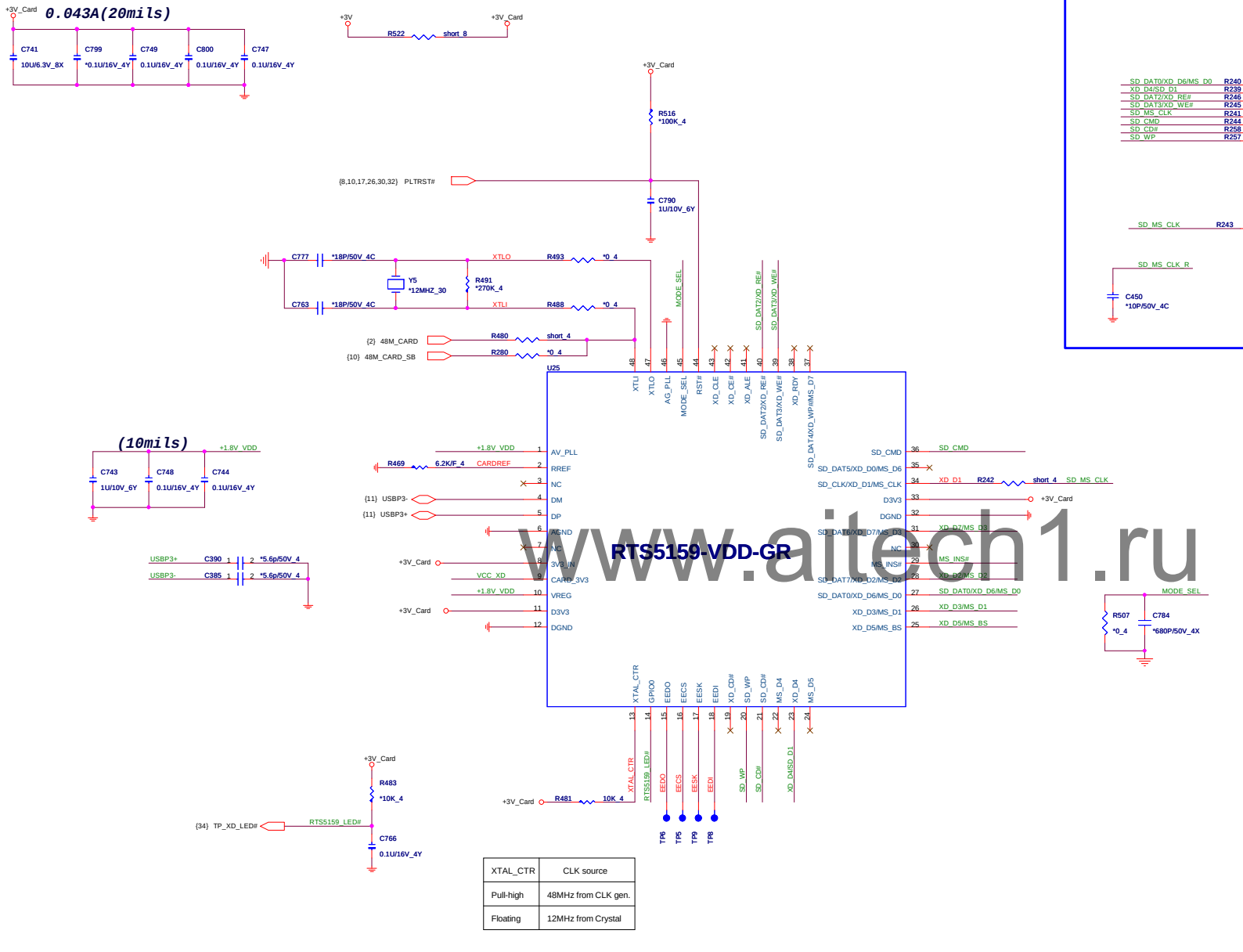
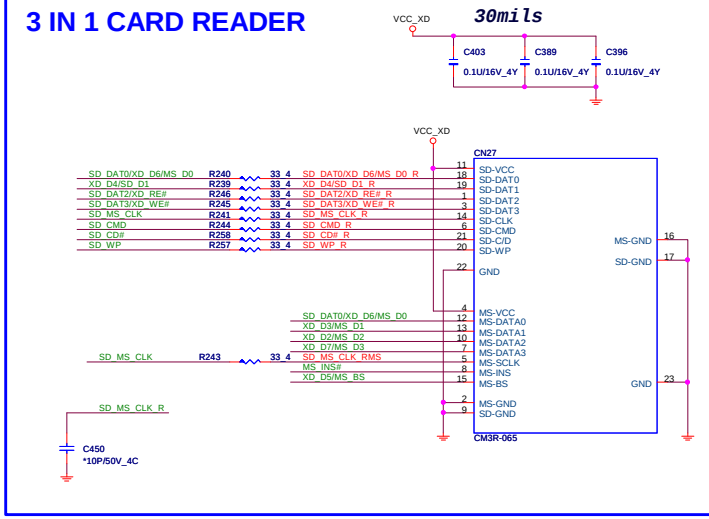
5 IN 1 CARD READER



RTS5159-VDD-GR

XTAL_CTR	CLK source
Pull-high	48MHz from CLK gen.
Floating	12MHz from Crystal

3 IN 1 CARD READER



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EC

0.03A(30mils) 0.03A(30mils) 0.01A(20mils)

H=1.6mm

WPCE775LA0DG

LPC: LFRAME, LAD0, LAD1, LAD2, LAD3, LCLK, CLKRUN/GPIO11, GA20, KBRST, ECSCI/GPIO54, LDRQ/GPIO24, LPCPD/GPIO10, LRESET, PWUREQ/GPIO67, SERIRQ, SMI/GPIO65

KB: KBSIN0–KBSIN7, KBSOUT0/JENK, KBSOUT1/TCK, KBSOUT2/TMS, KBSOUT3/TDI, KBSOUT4/JEN0, KBSOUT5/TDO, KBSOUT6/RDY, KBSOUT7–KBSOUT17/GPIO57

SMB: SCL1/GPIO17, SDA1/GPIO22, SCL2/GPIO73, SDA2/GPIO74, SCL3/GPIO23, SDA3/GPIO31, SCL4/GPIO47, SDA4/GPIO53

PS/2: PSCLK1/GPIO37, PSDAT1/GPIO35, PSCLK2/GPIO26, PSDAT2/GPIO27, PSCLK3/GPIO25, PSDAT3/GPIO12

A/D: AD0/GPI90, AD1/GPI91, AD2/GPI92, AD3/GPI93, AD4/GPIO05, AD5/GPIO04, AD6/GPIO03, AD7/GPIO07

D/A: DA0/GPI94, DA1/GPI95, DA2/GPI96, DA3/GPI97

GPIO: GPIO41(VBAT), GPIO42/TCK, GPIO43/TMS, GPIO44/TDI, GPIO50/TDO, CIRTX2/GPIO52/RDY

wake-up capability

no wake-up capability: GPO82/TRIS, GPO84/BADDR0

SER: SOUT_CR/GPO83/BADDR1, SIN_CR/CIRRX/GPIO87, GPIO06

PWM: A_PWM/GPIO15, B_PWM/GPIO21, C_PWM/GPIO13, D_PWM/GPIO32, E_PWM/GPIO45, F_PWM/GPIO40/CLKIN48, G_PWM/GPIO66, H_PWM/GPIO33

TIMER: TA1/GPIO56, TB1/GPIO14, TA2/GPIO20, TB2/GPIO01, TA3/GPIO51, TB3/GPIO36

SPI: SPI_CS1/GPIO64, SPI_DO/GPIO76/SHBM, SPI_SCK/GPIO75, GPIO81

FIR: IRRX1/GPIO72/SIN2, IRRX2_IRSL0/GPIO70, IRTX/GPIO71/SOUT2, CIRRXM/GPIO46/TRST

CIR: GPIO34/CIRRXL, CIRTX1/GPIO16, CIRTX2/GPIO30

FIU: F_SDI/F_SDIO1, F_SDO/SDIO0, F_CS0, F_SCK

CLKOUT/GPIO55, VCC_POR, VREF, 32KX1/32KCLKIN, 32KX2

Power pins: VCC1 19, VCC2 46, VCC3 78, VCC4 89, VCC5 115, AVCC 102, VDD 4, GND1 5, GND2 18, GND3 45, GND4 73, GND5 88, GND6 116, AGND 103, VCORF 44

Key components: Y2 32.768KHZ_10, C355 15P/50V_4C, C380 15P/50V_4C, R180 20M_6, R183 33K/F_4, R174 short_4, R181 short_4, R461 *0_4, L64 0_6, C304 1U/10V_6X, C442 0.1U/16V_4Y, C436 10U/6.3V_8X, C401 0.1U/16V_4Y, C407 10U/6.3V_8X, R202 short_6, C300 10U/6.3V_8X, C428 0.1U/16V_4Y, C359 0.1U/16V_4Y, C381 0.1U/16V_4Y, C342 0.1U/16V_4Y, C307 0.1U/16V_4Y, R131 2.2_6, L28 PBY160808T-601Y-N_1A, R492 *100K/F_4, R198 100K_4, R188 4.7K_4, R219 0_4, R727 10K_4, D7 SW1010CPT_100MA, R718 IV@10K_4, R719 EV@10K_4, TP10, TP4, TP1, D16 SW1010CPT_100MA, R658 *0_4

Signals: LFRAME#, LAD0–LAD3, PCLK_591, CLKRUN#, GATEA20, RCIN#, SCI#, EC_FPBACK#, PLTRST#, USB_EN#0, SERIRQ, BAT_SAT1, MX0–MX7, MY0–MY17, MBCLK, MBDATA, 2ND_MBCLK, 2ND_MBDATA, 3ND_MBCLK, 3ND_MBDATA, 3G_EN, HWPG, TPCLK, TPDATA, S3_Reduce, 2.5V_EN, USB_EN#1, LAN_P, CRT_SENSE#, 8768_32KX1, 8768_32KX2, RTCCLK_R, TEMP_MBAT, ICMNT, AC SET_EC, NBSWON#, Cell_separate, VFAN1, SUSLED_EC, BAT_SAT0, RF_LED, AMP_MUTE#, ID, D/C#, DISPON, WMAX_P, BADDR0, TP_ON_OFF, LID591#, CONTRAST, HWPG_VGA, CCD_POWERON, USBOC#13, SUSON, MAINON, BT_POWERON, PWRLED#, 3G_P, FANSIG1, ACIN, S5_ON, VRON, BT_RESET, BT_EN, ODD_EN, DNBSWON#, RSMRST#, SUSC#, MPWROK, BT_RFCTRL, NUMLED, CAPSLED, SPI_SDI_uR, SPI_SDO_uR, SPI_CS0#_uR, SPI_SCK_uR, VCC_POR#, VREF_uR, SUS_PWR_ACK, HWPG_2.5V

SM BUS PU

MBCLK	R166	4.7K_4
MBDATA	R156	4.7K_4
2ND_MBCLK	R136	4.7K_4
2ND_MBDATA	R135	4.7K_4
3ND_MBCLK	R224	4.7K_4
3ND_MBDATA	R225	4.7K_4

I/O Base Address

BADDR1-0	I/O Address	
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

BADDR0 R223 *10K_4; BADDR1 R495 10K_4; SHBM RF_EN R470 10K_4

ID

U5 M24C08-WMN6TP; 2ND_MBCLK, 2ND_MBDATA; C308 0.1U/16V_4Y

0.003A(20mils)

ADDRESS: A0H

SPI FLASH

U10 W25Q16BVSSIG; SPI_SDI_uR R201 33_4 SPI_SDI; SPI_SDO_uR R234 33_4 SPI_SDO; SPI_SCK_uR R235 33_4 SPI_SCK; SPI_CS0#_uR; R204 10K_4; C441 0.1U/16V_4Y

0.025A(20mils)

INTERNAL KEYBOARD STRIP SET

MY0 R133 10K_4

HWPG

{42} VGPU_IO_PG D18 *EV@SW1010CPT_100MA; {22} +1.8V_GPU_PWGD D14 *EV@SW1010CPT_100MA HWPG_VGA; R226 10K_6

Intel {36} SYS_HWPG D9 SW1010CPT_100MA; Intel {38} HWPG_1.05V D15 SW1010CPT_100MA; AMD {38} HWPG_NB_CORE; Intel {37} HWPG_1.5V D8 SW1010CPT_100MA; Intel {39} HWPG_VTT D12 SW1010CPT_100MA; AMD {39} +1.1V_HWPG; R160 10K_6 HWPG

SMBUS Table

SMBUS	Devices	Address
1	Battery	
2		
	PCH SML1	
	AMD SMBus	98H
	EC EEPROM	A0H
3	VGA Board Thermal Sensor	98H

DNBSWON# C405 *0.1U/16V_4Y; NBSWON# SW1 *SHORT_PAD; D17 *EGA10402V05AH; PCLK_591 R209 *22_4 C421 *10P/50V_4C; R458 10K_4 TPCLK; R454 10K_4 TPDATA; AC SET_EC C437 *10U/6.3V_8X; ICMNT C438 *10U/6.3V_8X; 8769AGND

LED PU/PD

PWRLED# R144 10K_4 R145 *10K_4; BAT_SAT0 R463 10K_4; BAT_SAT1 R479 10K_4

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	EC-WPC8763LDG/WPC8769L(O)	D3A

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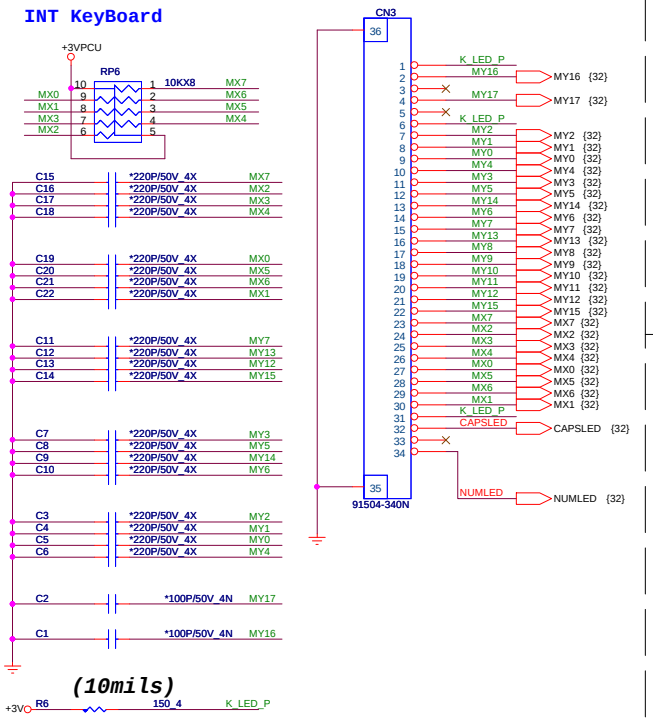
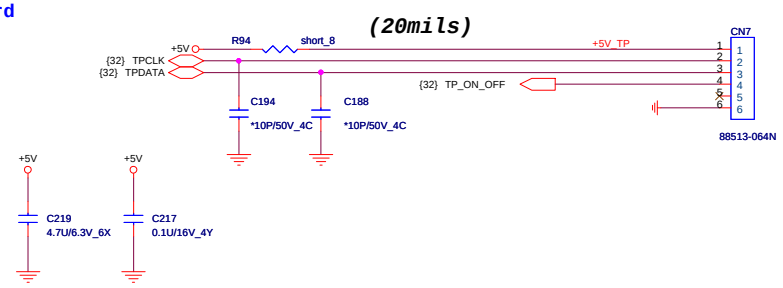
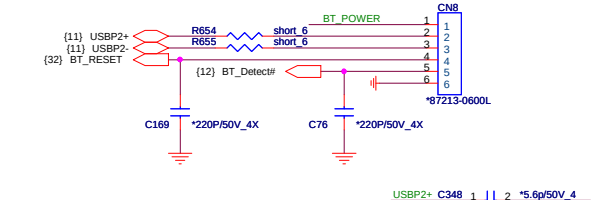
INT KeyBoard

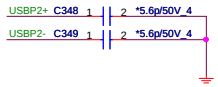


TP board

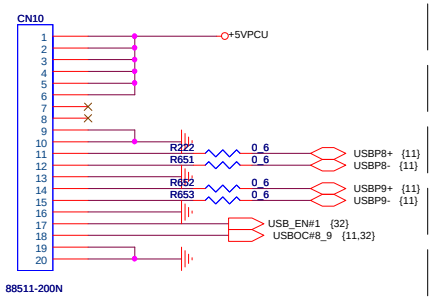


Bluetooth

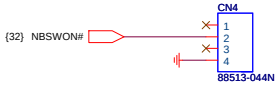


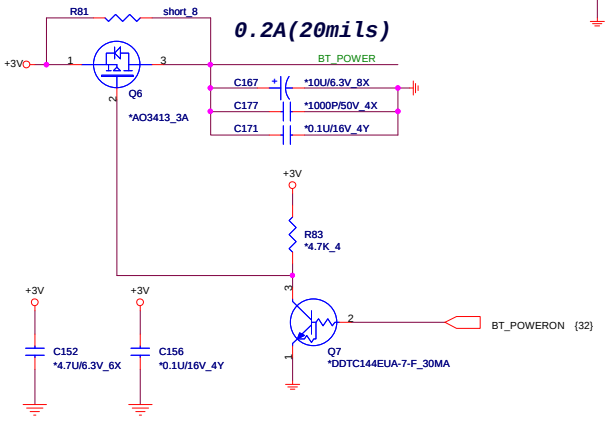


USB board



Power board





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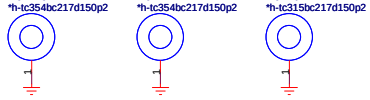
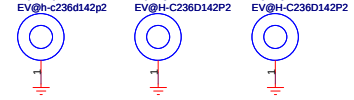
NUT

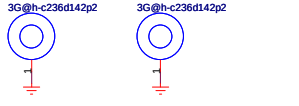
CPU



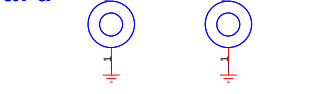
VGA



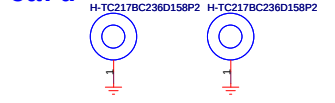
SIM



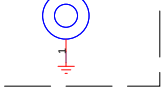
3G Card



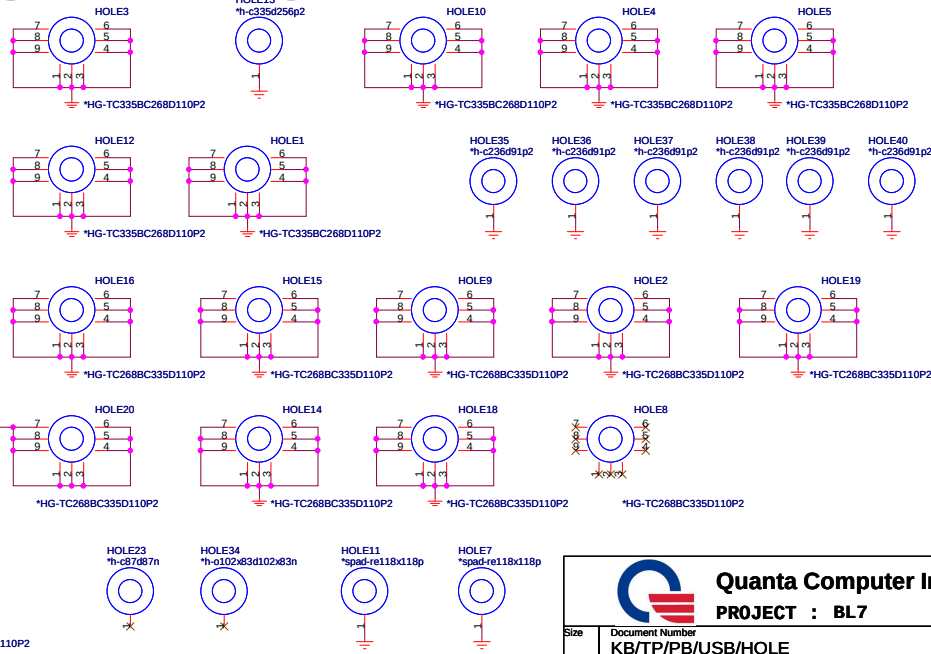
WLAN Card



MOD



HOLE



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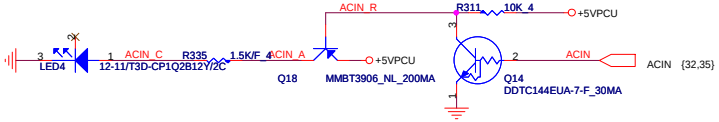
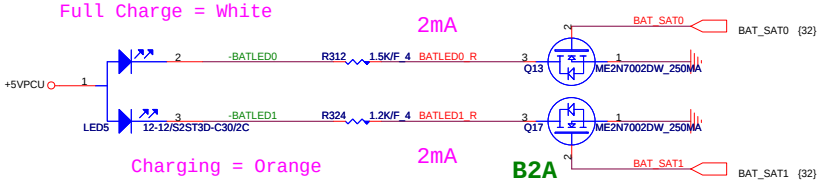
LED

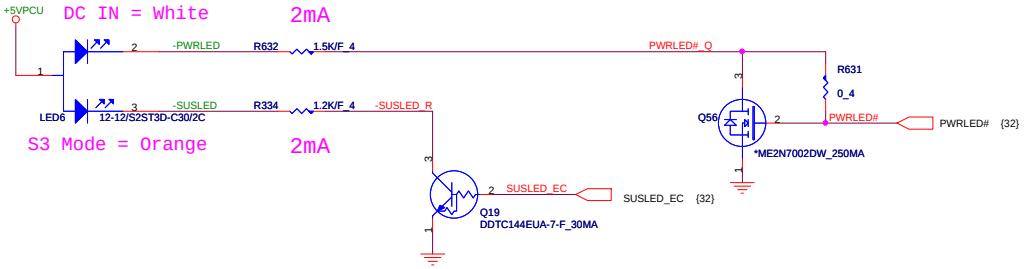
AC-IN



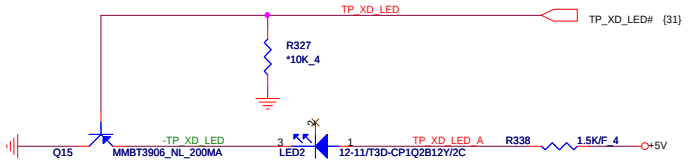
BATERRY



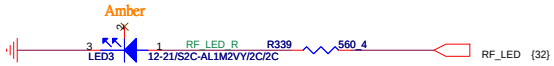
POWER



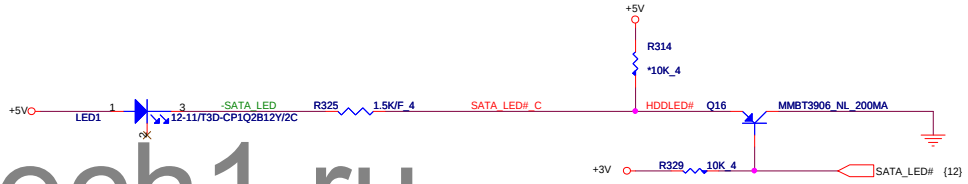
CARDREADER



RF LED



HDD/ODD



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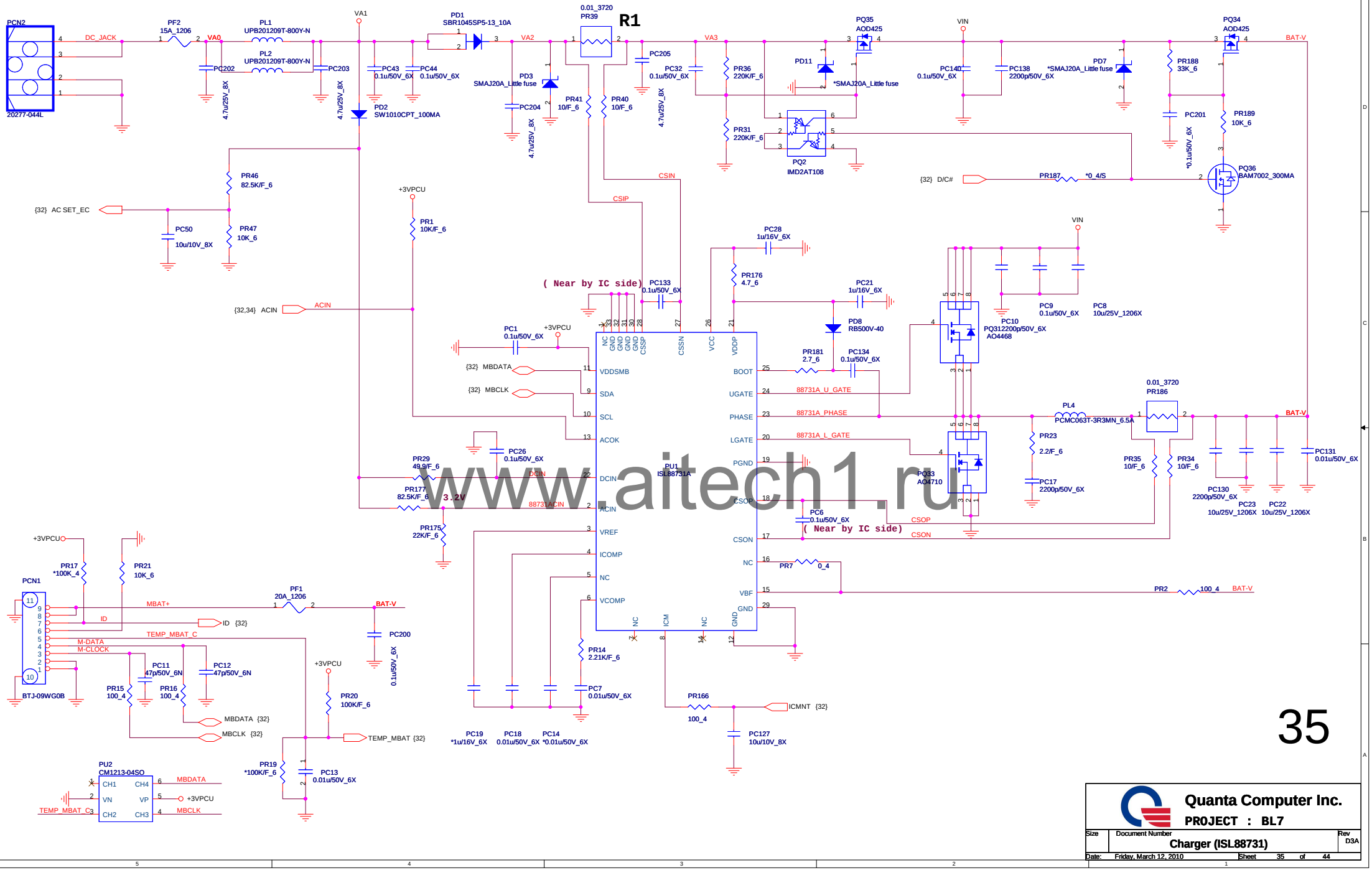
ESD Protect

Quanta Computer Inc.		
PROJECT : BL7		
Size	Document Number: LED	Rev: D3A
Date: Friday, March 12, 2010	Sheet 34 of 44	



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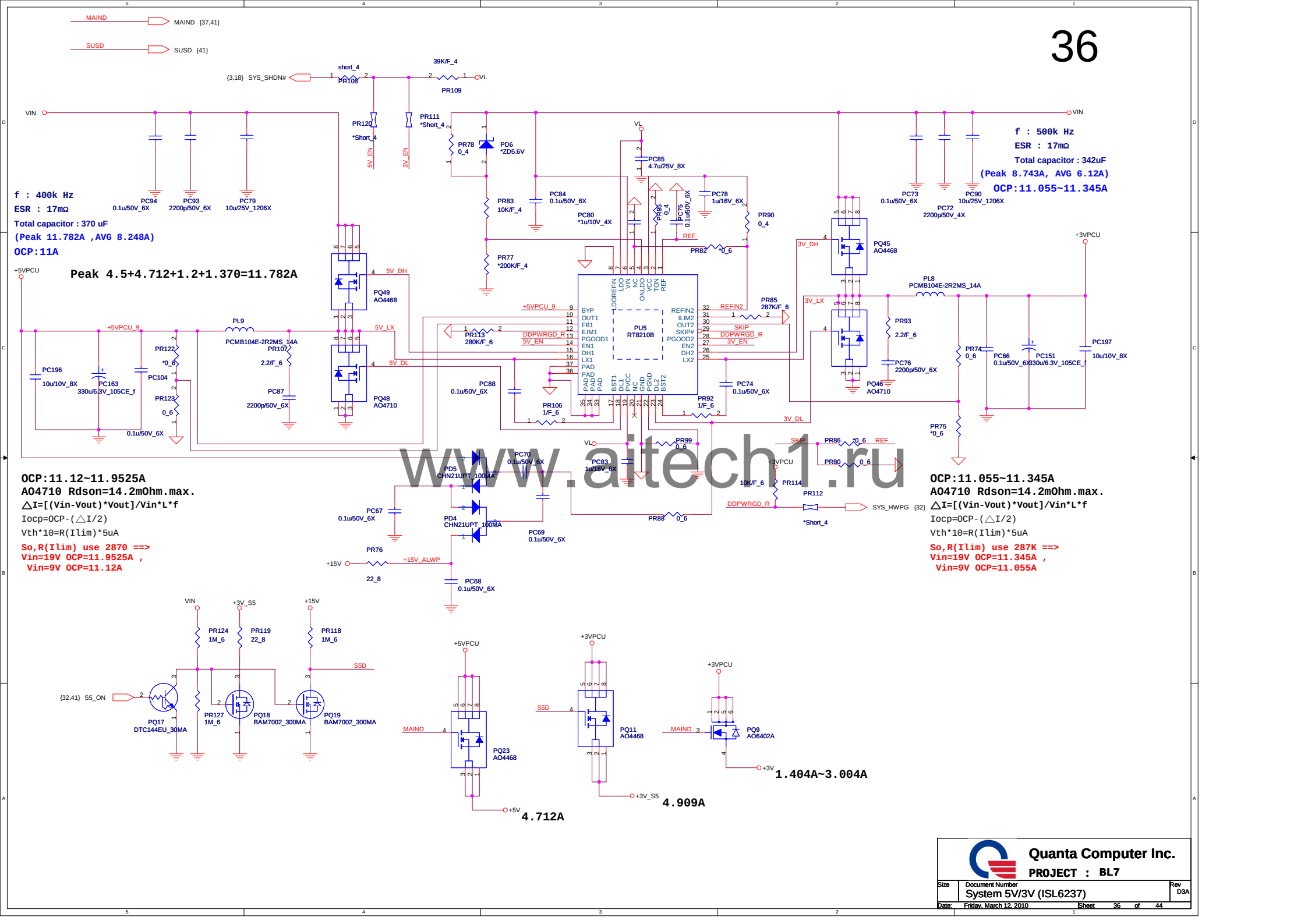
Quanta Computer Inc.
PROJECT : BL7

Size	Document Number	Rev
	Charger (ISL88731)	D3A

Date: Friday, March 12, 2010 Sheet 35 of 44



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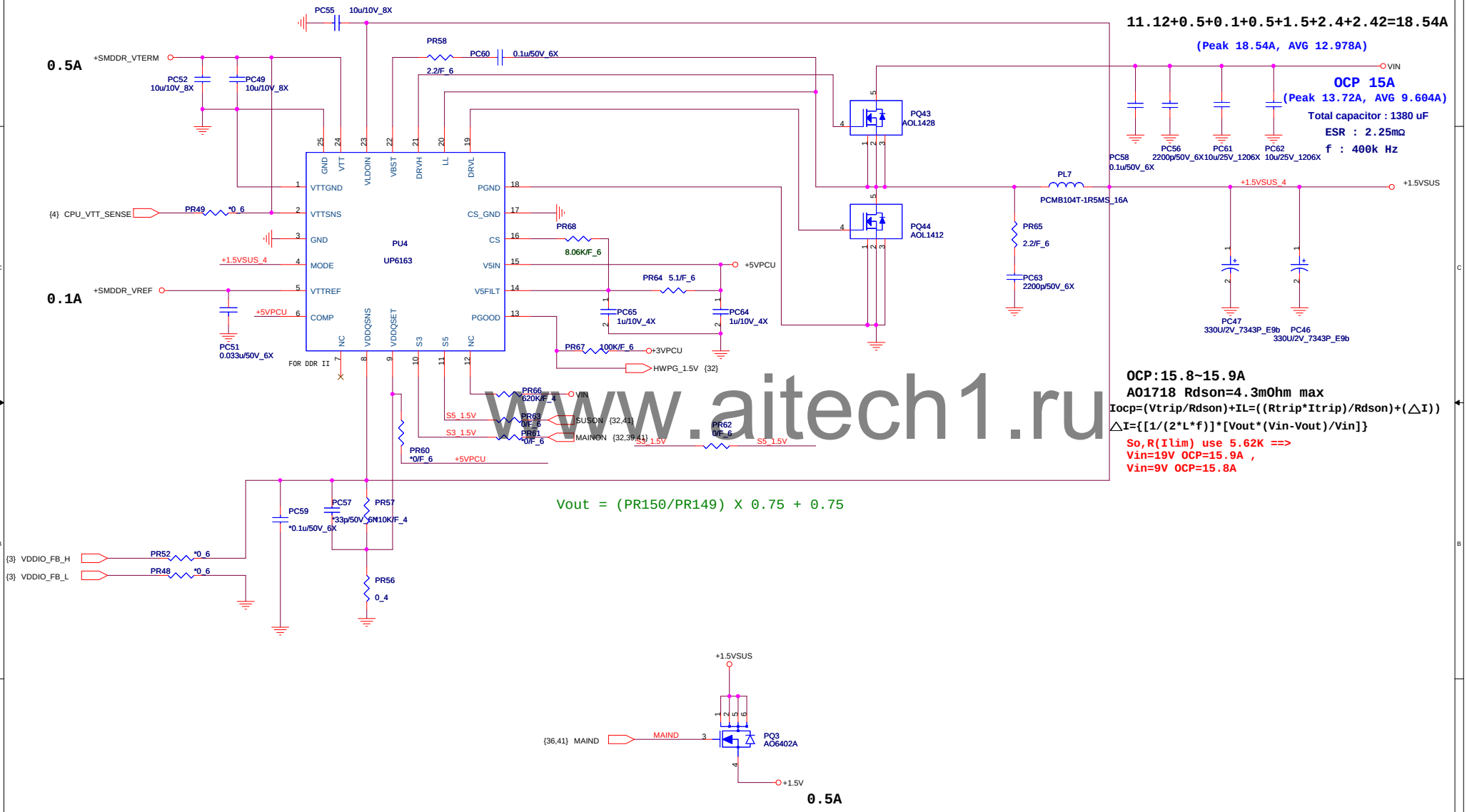
Quanta Computer Inc.
PROJECT : BL7

Size	Document Number	Rev
	System 5V/3V (ISL6237)	D3A
Date: Friday, March 12, 2010	Sheet 36 of 44	



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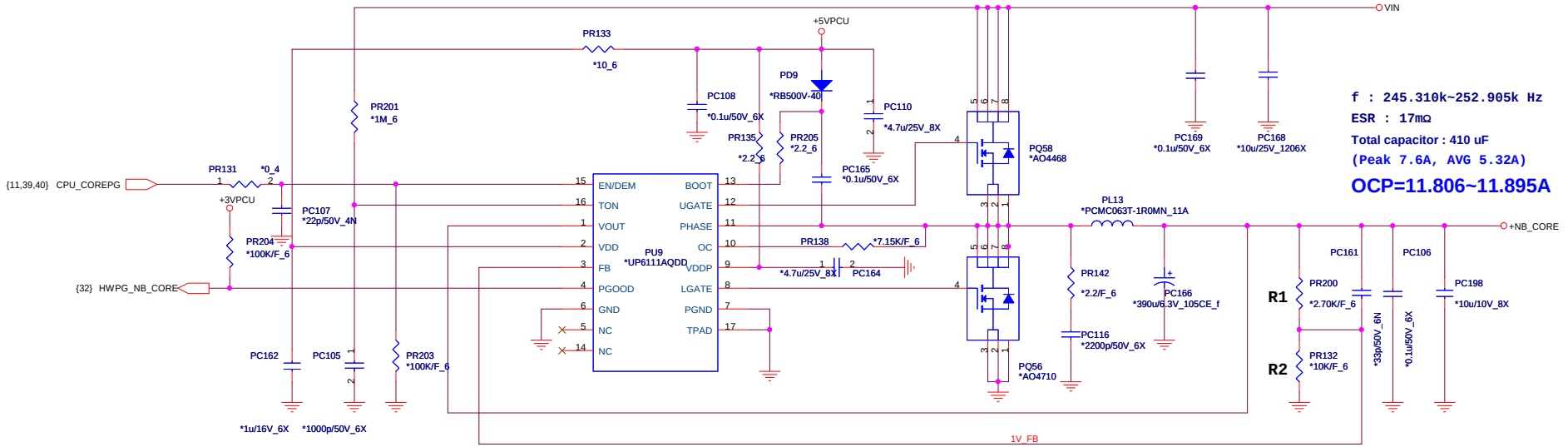
PROJECT : BL7

Size	Document Number	Rev
	DDR 1.5V (UP6163)	D3A

Date: Friday, March 12, 2010 Sheet 37 of 44



f : 245.310k~252.905k Hz
ESR : 17mΩ
Total capacitor : 410 uF
(Peak 7.6A, AVG 5.32A)

OCP=11.806~11.895A

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Vout=0.75*[1+(R1+R2)]

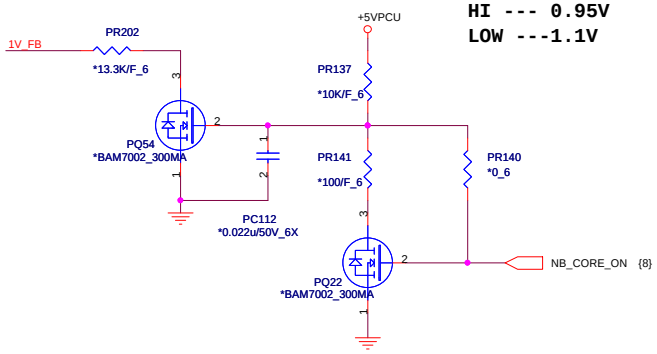
Ton=3.85p*Rton*Vout/(Vin-0.5) F=Vout/(Vin*Ton)

AO4710 Rdson=14.2mOhm.max.

Ripple current=((Vin-Vo)/f*L)*(Vo/Vin)

OCP =(Rimax*20uA/LRdson)+(Ripple/2)

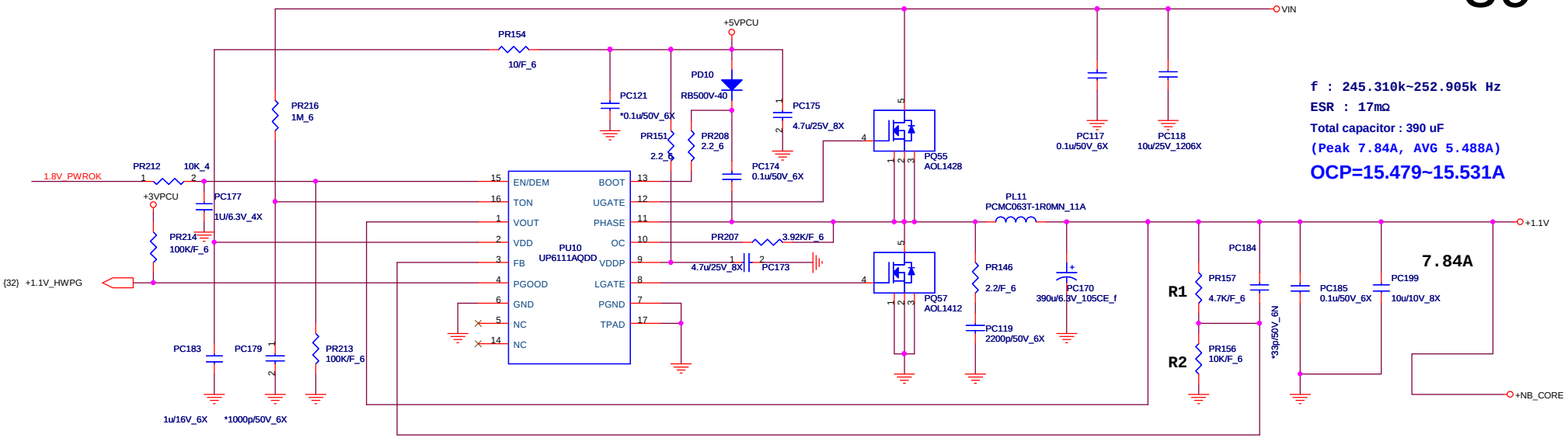
Vout=0.75*[1+(R1+R2)]



R2=10KΩ,R1=2.7KΩ

So,Vin=19V==>
OCP=11.895A;
Vin=9V==>
OCP=11.806A

Quanta Computer Inc.		
PROJECT : BL7		
Size	Document Number: NB_CORE (UPI6111)	Rev: D3A
Date: Friday, March 12, 2010	Sheet 38 of 44	



Vout=0.75*[1+(R1+R2)]
Ton=3.85p*Rton*Vout/(Vin-0.5) F=Vout/(Vin*Ton)
AO4710 Rdson=14.2mOhm.max.
Ripple current=((Vin-Vo)/f*L)*(Vo/Vin)
OCP =(Rimax*20uA/LRdson)+(Ripple/2)
Vout=0.75*[1+(R1+R2)]

R2=10KΩ,R1=4.7KΩ
So,Vin=19V==>
OCP=15.531A;
Vin=9V==>
OCP=15.479A

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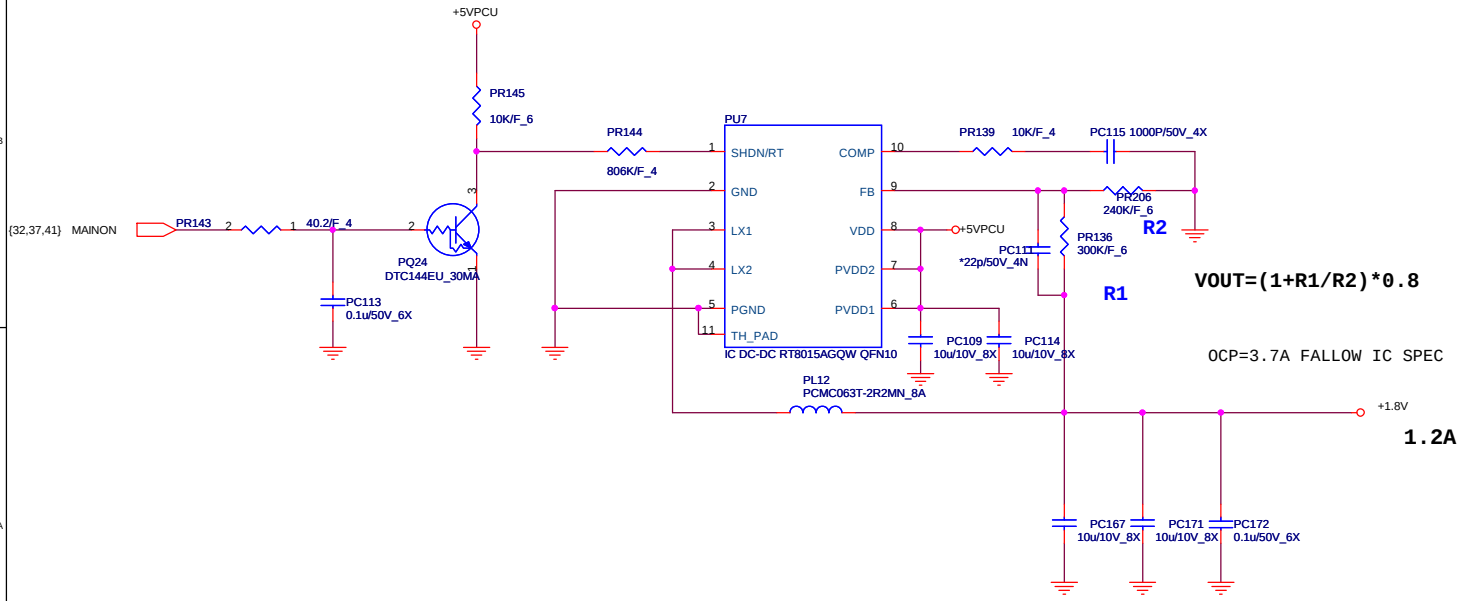

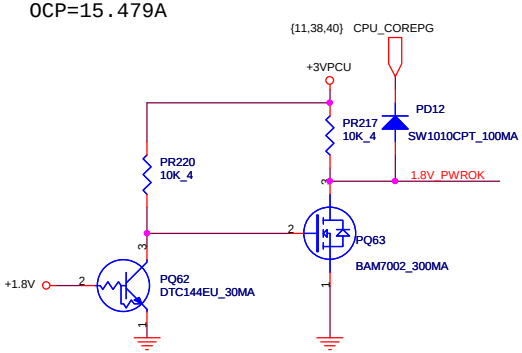

Quanta Computer Inc.		
PROJECT : BL7		
Size	Document Number: +1.1V/+1.8V (UP6111)	Rev: D3A
Date: Friday, March 12, 2010	Sheet 39 of 44	

VDDNB Core(Peak 4A,AVG 2.8A) OCP 4.5A

OCP_NB=ROCSET*10uA/Rdson

ROCSET=PR34

OCP_NB=11.3k*10uA/23m=4.91A

Total capacitor : 370 uF

ESR : 9mΩ

f : 300k Hz

4A

OFS/VFIXEN	Offset & Droop	SVI	VFIX
GND	O	O	X
+3.3V	X	X	O
+5V	X	O	X

Metal VID Codes

SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

Pin 49 is GND Pin

PU3 ISL6265A

Total capacitor : 1404.4 uF

ESR : 2.25mΩ

f : 300k Hz

Core (Peak 20A,AVG 16A)

OCP 28A

46A

B TEST DEL JP 13

OCP 28A

VOSET=1.17V*Rocset/(Rbias+Rocset)

Ioc=VOCSET/30/(K*DCR*1.4)

K=PR33/(PR33+PR32)

VOSET=1.17V*107/(107+10)=1.07V, K=18.2/(18.2+3.92)=0.822

Ioc=1.07V/30/(0.822*1.1m*1.4)=28.175A.

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PROJECT : BL7

Size | Document Number: AMD CPU Core (ISL6265A) | Rev: D3A

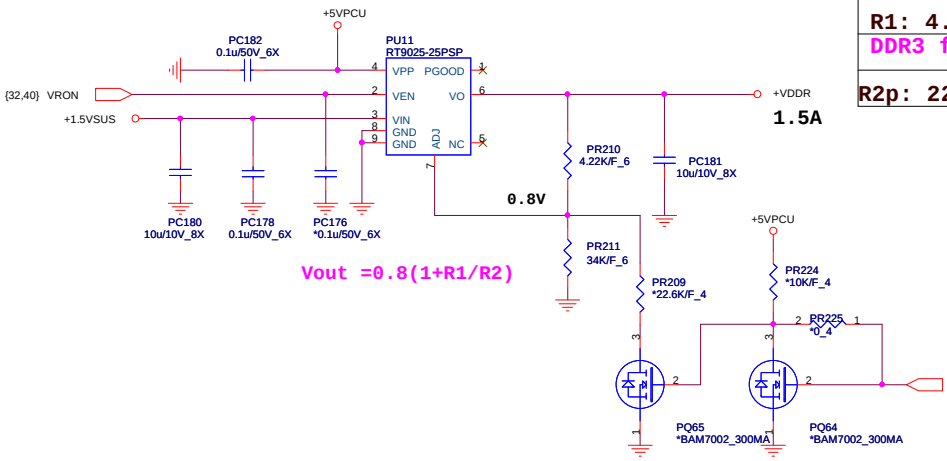
Date: Friday, March 12, 2010 | Sheet 40 of 44

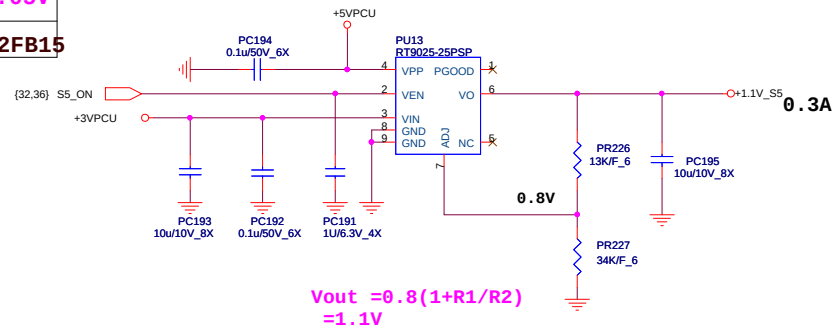
DDR3 for 1066MHZ----0.9V

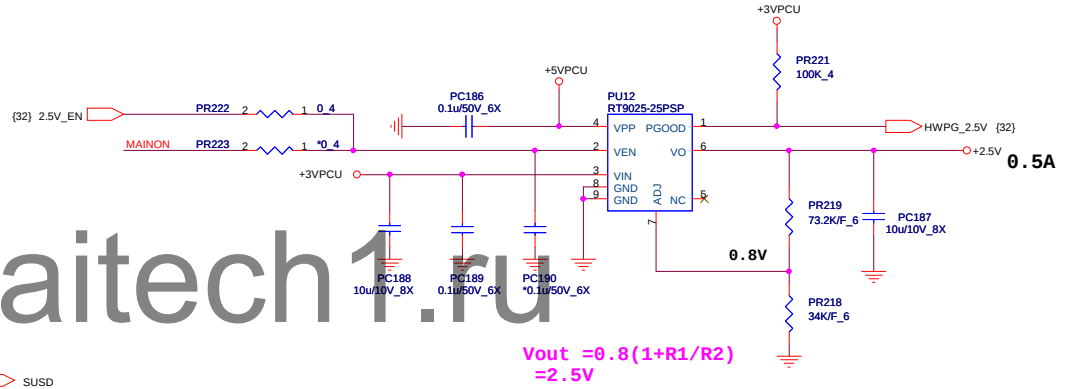
R1: 4.22K/F_6: CS24223F917

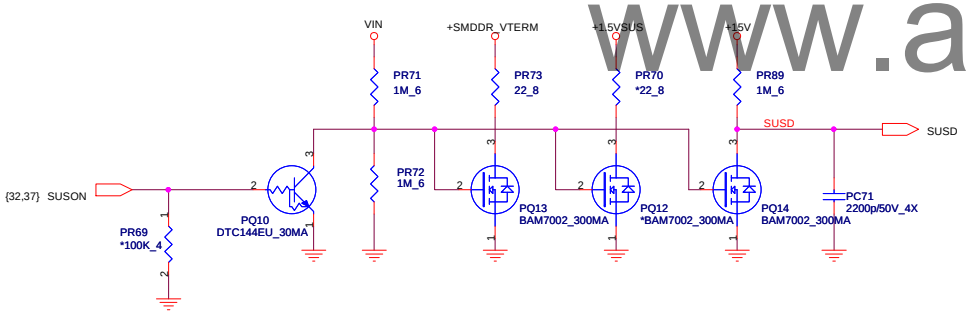
DDR3 for 1333MHZ----1.05V

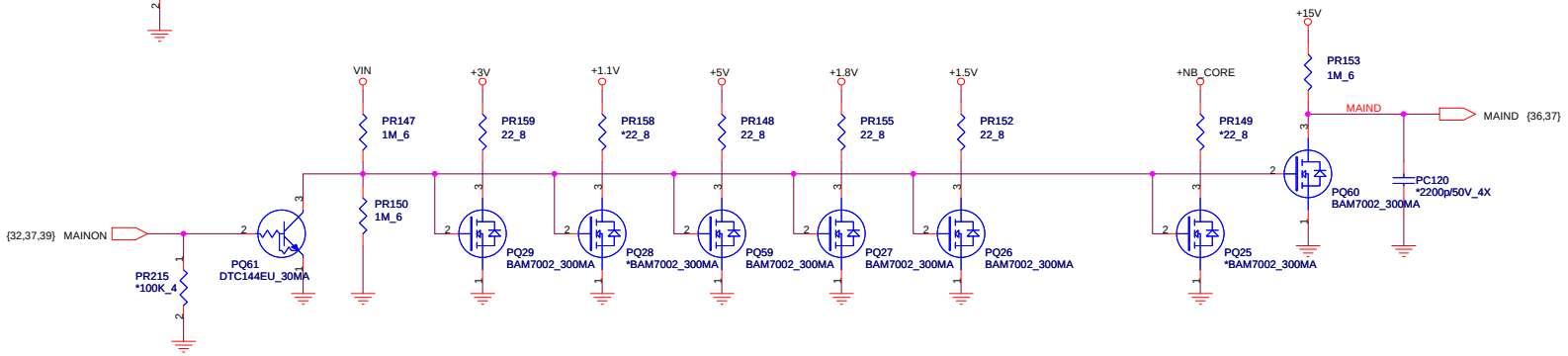
R2p: 22.6K/F_4: CS32262FB15











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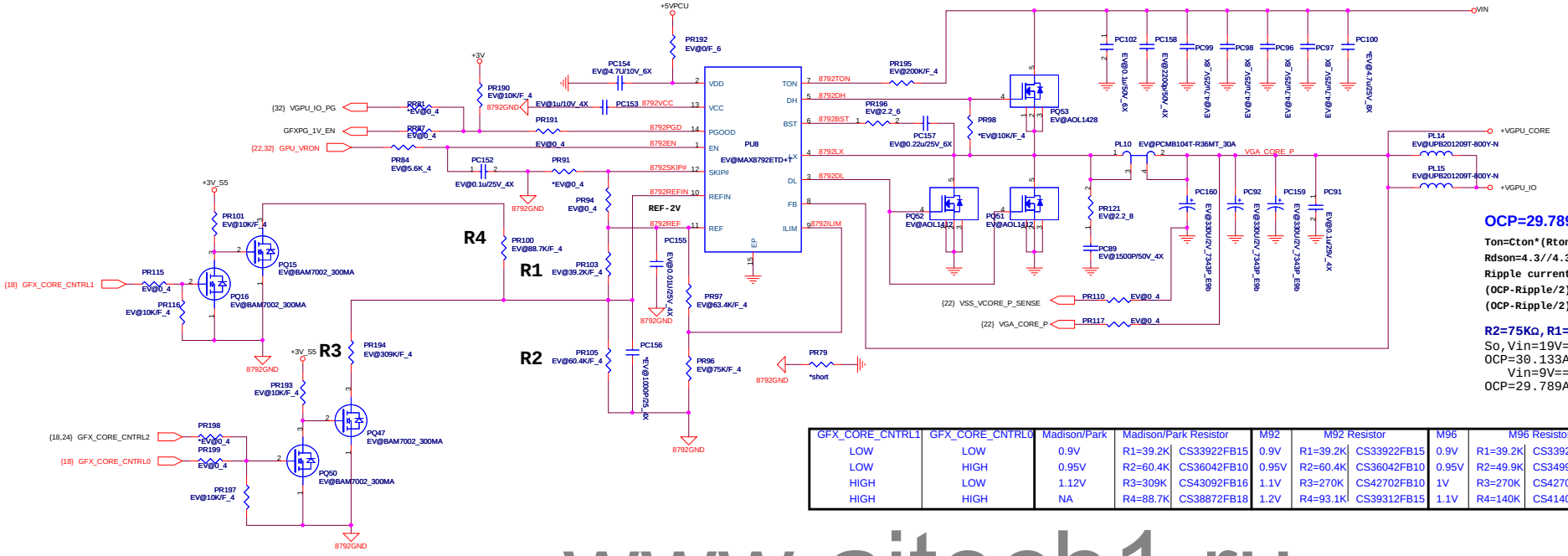
Quanta Computer Inc.

PROJECT : BL7

Size	Document Number	Rev
	Discharge/2.5/1.1/VDDR	D3A

Date: Friday, March 12, 2010 Sheet 41 of 44



OCP=29.789~30.133A

(Peak 28A, AVG 23.1A)

Total capacitor : 1400 uF

ESR : 2.25mΩ

F: 297k Hz

OCP=29.789~30.133A

Ton=Cton*(Rton+6.5k)*(Vfb/Vout),F=297kHz
Rdson=4.3//4.3=2.15mΩ
Ripple current=((Vin-Vo)/f*L)*(Vo/Vin)
(OCP-Ripple/2)=25.57
(OCP-Ripple/2)*Rds=Vref*((R2/(R1+R2))/20)

R2=75KΩ,R1=63.4KΩ

So,Vin=19V==>
OCP=30.133A;
Vin=9V==>
OCP=29.789A

GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	Madison/Park	Madison/Park Resistor		M92	M92 Resistor		M96	M96 Resistor	
LOW	LOW	0.9V	R1=39.2K	CS33922FB15	0.9V	R1=39.2K	CS33922FB15	0.9V	R1=39.2K	CS33922FB15
LOW	HIGH	0.95V	R2=60.4K	CS36042FB10	0.95V	R2=60.4K	CS36042FB10	0.95V	R2=49.9K	CS34992FB10
HIGH	LOW	1.12V	R3=309K	CS43092FB16	1.1V	R3=270K	CS42702FB10	1V	R3=270K	CS42702FB10
HIGH	HIGH	NA	R4=88.7K	CS38872FB18	1.2V	R4=93.1K	CS39312FB15	1.1V	R4=140K	CS41402FB14

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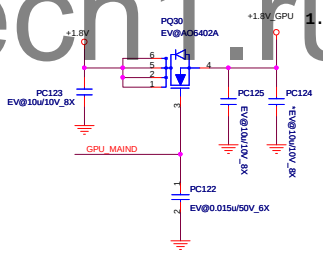
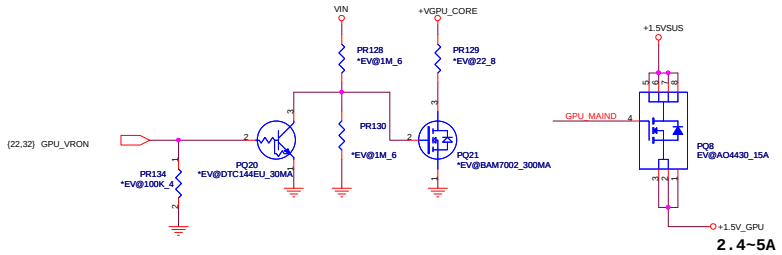
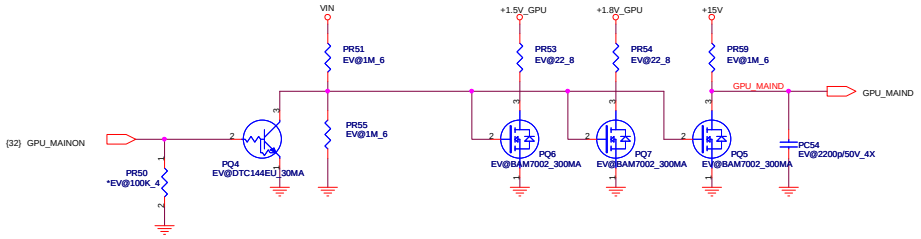
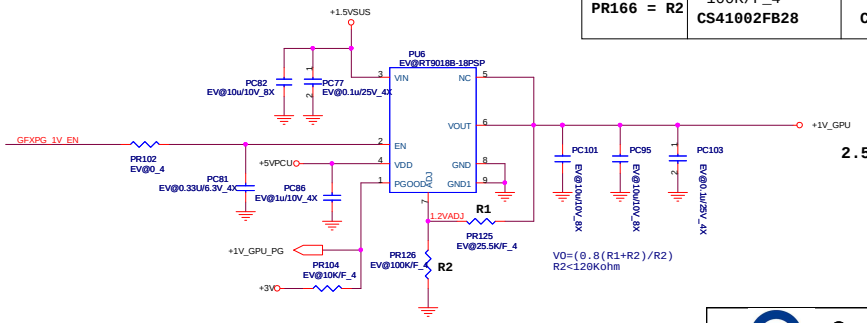






PCIE_VDDC
M92,M96-->1.1V
Madison,Park-->1.0V

	Madison,Park	M92,M96
PR163 = R1	25.5K/F_4 CS32552FB11	38.3K/F_4 CS33832FB08
PR166 = R2	100K/F_4 CS41002FB28	100K/F_4 CS41002FB28



VO=(0.8(R1+R2)/R2)
R2<120Kohm

Quanta Computer Inc.
PROJECT : BL7

Size	Document Number	Rev
	+VGPU_CORE (MAX8792)	D3A
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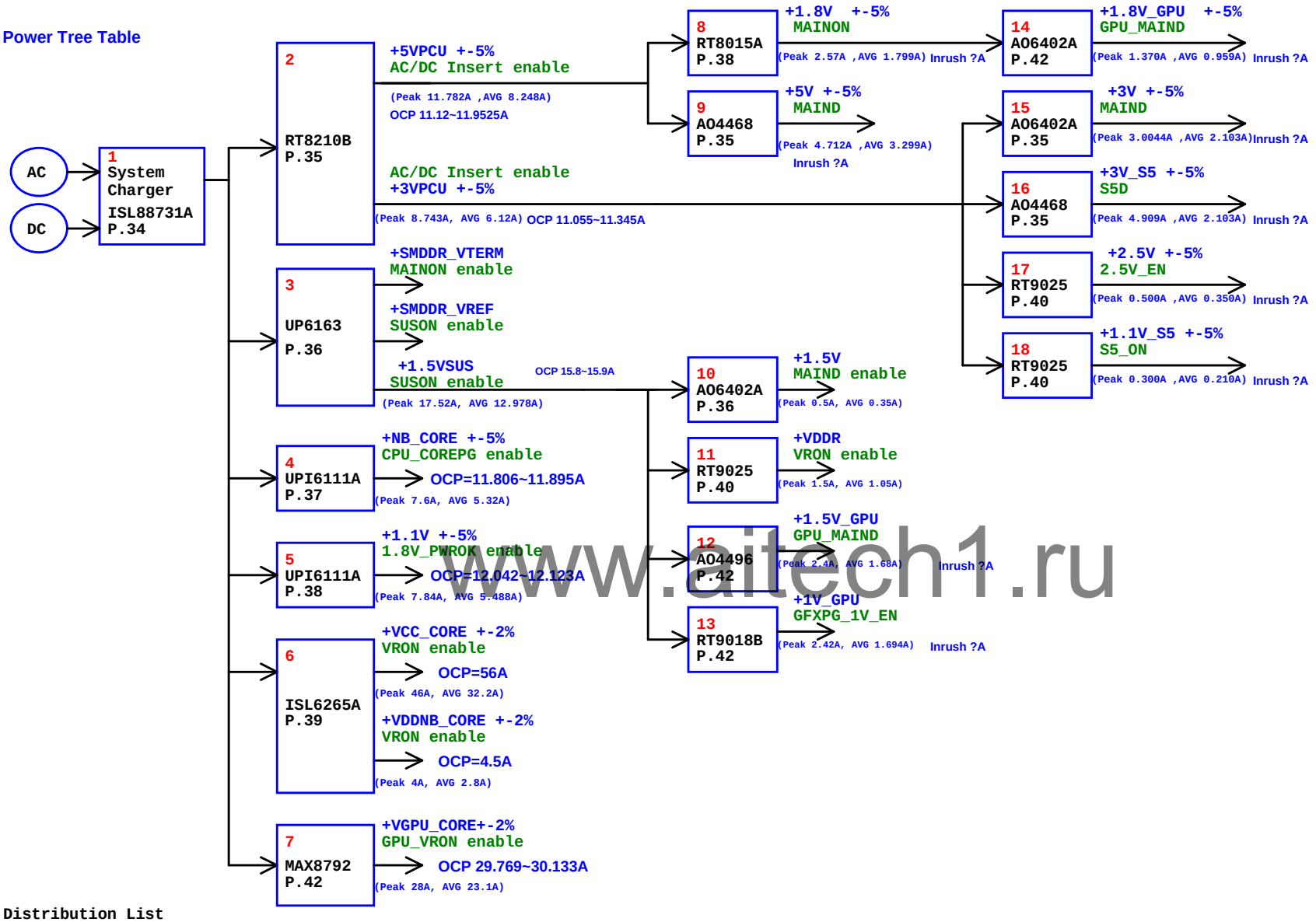
Power Tree Table



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Power Distribution List

Power	Distribution

Model	REV	CHANGE LIST
BL7 MB	B1B	PAGE 2 : Change RP18 Value and Add R722 for VGA SKU,Change RP20 Value for 3G,and change R187 to SEL_HT66
		PAGE 3 : Mount R24,and Add Q58,R639,D47 and del R372,R33,Q5 for VGA Therm Detec
		PAGE 6 : Mount C78,C113,C569,C570,C28 for EMI request
		PAGE 11 : Add Board ID7 and Board ID8 and R644,R645,R646, and del R136 and change R578,R575,R559 for AMD suggestion
		PAGE 14 : Mount R573 and Del R572 for Gen I mode
		PAGE 18 : Change CTR port for Madison,Park,M92,M96 co-lay
		PAGE 19 : Change R546 value to 51 ohm port for Madison,Park,M92,M96 co-lay
		PAGE 22 : Delete reserve C423,C429,C427,C417,C430,C433,C422,C390,C409,C361,C376,C362,C378,C348,C349,C385,C374,C340,C352,C367,C350 for layout placement
		PAGE 22 : Add L73,L74,C896,C897,R723,R724,L72,R713,R711,R712R709 for Madison,Park,M92,M96 co-lay
		PAGE 23 : Add R714,R715,R716 for Madison,Park,M92,M96 co-lay
		PAGE 24 : Add U0,R720,R721,C895,R717 for Madison,Park,M92,M96 co-lay
		PAGE 25 : Change R1&R2 to bead for EMI request
		PAGE 26 : Add Q67,R735,R732,R736 for WLAN & BT Combo Module
		PAGE 27 : Del F2
		PAGE 30 : Add R636,R637,R635,R729,Q59,R734,R725,C899,C900,C619 for non over clocking
		PAGE 32 : Add R718,R719 for 3 cell Battery protect
		PAGE 33 : Add R222,R651,R652,R653 for EMI request
		PAGE 39 : Change PR207 to 3.92Kohm for OCP setting
		PAGE 39 : change PQ55,PQ57 footprint for higher current requirement
		PAGE 39 : Add PC199 for EMI
	C3A	PAGE 2 : Change RP13,RP14,RP15,RP16,RP17,RP21 to shortpad,RP22,And Change CLKREQ3#/CLKREQ4# netname to PCIE_CLK_REQ4#/PCIE_CLK_REQ3#
		PAGE 3 : Change R22,R90,R105,R120,R359,R34,R93,R42,R45 to shortpad,And Change T9,T10 Footprint and change R28 value,and mount R372,Q58,And del D25,D47,R368,R373,Q27,CN5,and Add Q65
		PAGE 7 : Change C594,C593 value
		PAGE 8 : Change R412,R402,R394,R423,R436,R413,R122 to shortpad
		PAGE 9 : Change R64,R75,L1,L5,L7,R87 to shortpad
		PAGE 10 : Change C843,C863,C870,C881 Value,and change R539 to shortpad
		PAGE 11 : Add R659 and change R247,R250,R141,R138 to shortpad,and mount R139,and del C885,U29
		PAGE 13 : Change R256,R262,R313,R310,R281,L42,L39 to shortpad
		PAGE 16 : Del R523,R519,R514,R508,R504,R496,R530,R527,R259,R260, and Add RN34,RN35,RN36,RN37,R496,R504,R508,R514 for EMI
		PAGE 17 : Change R100 to shortpad
		PAGE 18 : Change R464,R445 to shortpad
		PAGE 24 : Change R717 to 0 ohm
		PAGE 25 : Change R347,R348,L43 to shortpad ,and mount Q55,Q57,and change R633 value and add D46 and del D45
		PAGE 26 : Change R192,R193 to shortpad
		PAGE 27 : Del C301
		PAGE 28 : Change R383 and R489 to shortpad
		PAGE 30 : Change R390,R382,R389,R381,and change C197,C198,R65,R59 Value
		PAGE 31 : Change R480,R522,R242 to shortpad
		PAGE 32 : Add R727,and change R174,R181,R202 to shortpad,and change C355,C380 value,and reverse R658
		PAGE 33 : Change R94,R81,R654,R655 to shortpad
		PAGE 35 : Add PC202,PC203,PC204,PC205,PC201 for EMI
		PAGE 36: CHange PR108 footprint to shortpad
		PAGE 37: Change PQ43,PQ44 Value
		PAGE 39: Change PQ55,PQ57,PR144,PL12,PR139 Value
		PAGE 40: Change PL3,PQ41,PQ39,PQ40,PQ37,PQ38 Value,and Add PC206
		PAGE 41: Reverse PR70,PQ12,PQ158,PQ28,PR149,PQ25
	D3A	PAGE 11 : Reverse R163 and change R584,R579,R576 Value to 0_4
		PAGE 12 : Reverse R534,Y6,C817,C808
		PAGE 13 : Reverse C904,C905
		PAGE 16 : Add F2 for HDMI Safety issue
		PAGE 27 : Reverse C23 and C340
		PAGE 29 : Add R660,R661,R662
		PAGE 34 : Change R335,R312,R338,R632,R325 value to 1.5K_4 for LED lightness issue

MODEL	BL7
PAGE	FROM / To
1	1A / 1B
2	1A / 1B
3	1A / 1B
4	1A / 1B
5	1A / 1B
6	1A / 1B
7	1A / 1B
8	1A / 1B
9	1A / 1B
10	1A / 1B
11	1A / 1B
12	1A / 1B
13	1A / 1B
14	1A / 1B
15	1A / 1B
16	1A / 1B
17	1A / 1B
18	1A / 1B
19	1A / 1B
20	1A / 1B
21	1A / 1B
22	1A / 1B
23	1A / 1B
24	1A / 1B
25	1A / 1B
26	1A / 1B
27	1A / 1B
28	1A / 1B
29	1A / 1B
30	1A / 1B
31	1A / 1B
32	1A / 1B
33	1A / 1B
34	1A / 1B
35	1A / 1B
36	1A / 1B
37	1A / 1B
38	1A / 1B
39	1A / 1B
40	1A / 1B
41	1A / 1B
42	1A / 1B
43	1A / 1B
44	1A / 1B
45	1A / 1B

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DOC NO. 204					
PROJECT MODEL :	BL7	APPROVED BY:	Eric Lai	DATE:	2010/03/11
PART NUMBER:	31BL7MB0010	DRAWING BY:	Eric Lai	REVISON:	D3A

Quanta Computer Inc.
PROJECT : BL7
Size | Document Number: EE change list | Rev: D3A
Date: Friday, March 12, 2010 | Sheet 44 of 44